

Selek 15" CML Schematic

CML-H

2019/05/29

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REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

Selek CMLH N18E



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Selek CML-H

Rev

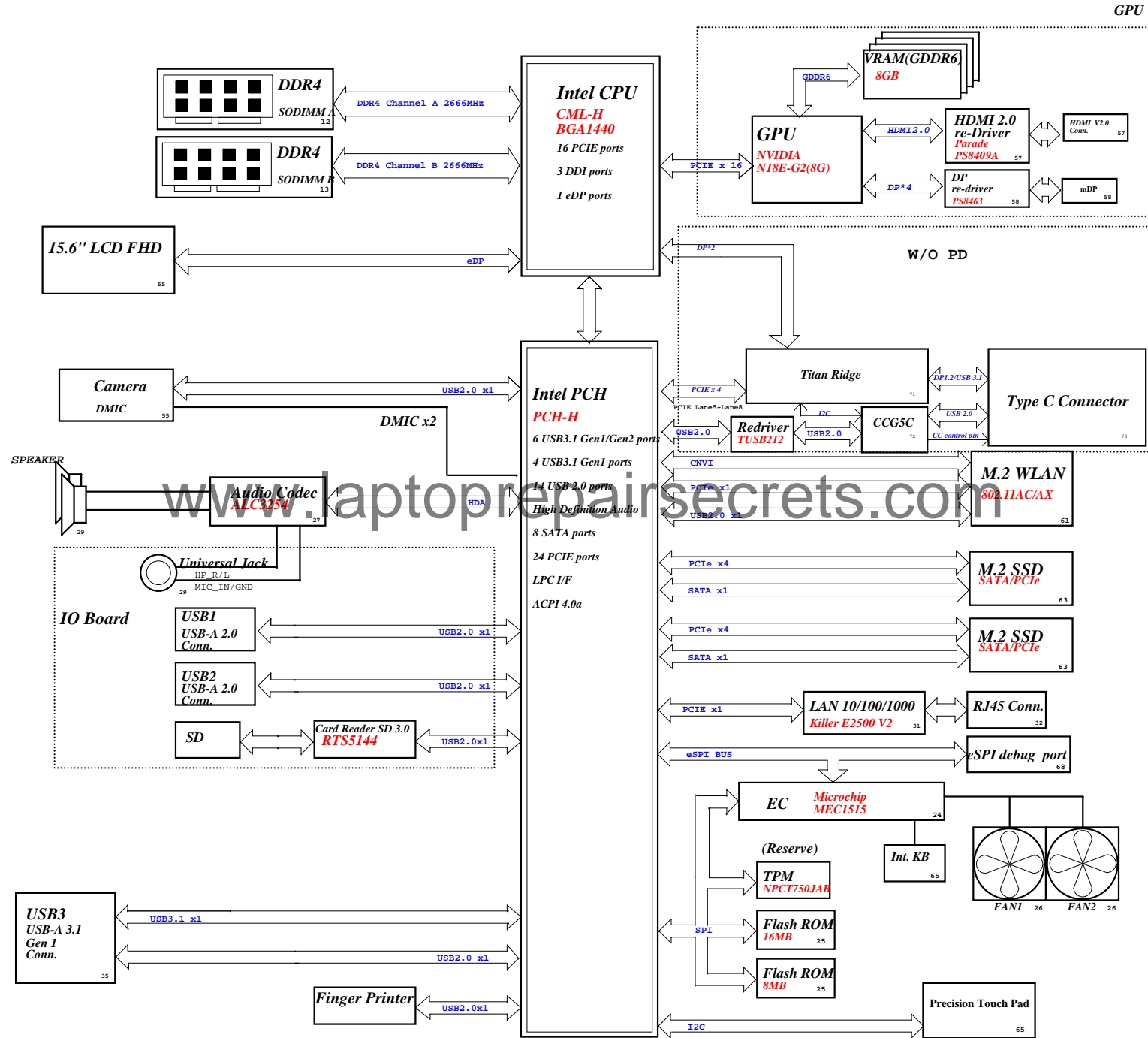
A00

Date: Sunday, June 21, 2020

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Project Code : 4910K7010001
PCB P/N : 19753-1
Revision : A00

Selek N18E



GPU

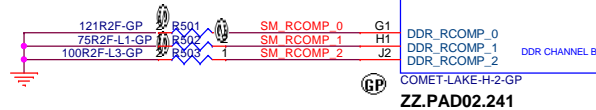
W/O PD

CHARGER		44
ISL88739		
INPUTS		OUTPUTS
AD+		DCBATOUT
BT+		
SYSTEM DC/DC		45
TPS51225RUKR-GP		
INPUTS		OUTPUTS
DCBATOUT		3D3V_PWR 3D3V_S5 5V_PWR 5V_S5
CPU Core Power		46-50
NCP81208MNTXG		
NCP81382MNTXG x 2		
NCP81382MNTXG (23e)		
NCP81253MNTBG		
INPUTS		OUTPUTS
DCBATOUT		VCC_CORE
DCBATOUT		+VCCGT
DCBATOUT		+VCCGT (23e)
DCBATOUT		+VCCSA
DDR4 SUS		51
RT8231AGQW-GP		
APL5930KAI-TRG		
INPUTS		OUTPUTS
DCBATOUT		1D2V_S3 0D6V_S0 2D5V_S3
CPU VCCPRIM_CORE		1V
1V		
INPUTS		OUTPUTS
1D0V_S5		+VCCPRIM_CORE
CPU DDC-VLD00A		53
AO22262QI-10-GP-U		
INPUTS		OUTPUTS
DCBATOUT		1D0V_S5
LDO-VLD8V		54
APL5930KAI-TRG		
INPUTS		OUTPUTS
3D3V_S5		1D8V_S5
5V/3V_S0		40
TPS22966DPUR-GP		
INPUTS		OUTPUTS
5V_S5 3D3V_S5		5V_S0 3D3V_S0
EOP10/EDRAM (23e)		40
TPS22961DNYT		
INPUTS		OUTPUTS
1D0V_S5 1D0V_S5		+V_EDRAM_VR +V_EOP10_VR
3D3V_VGA		86
AO3419L		
INPUTS		OUTPUTS
3D3V_S0		3D3V_VGA_S0
VGA_CORE		85
ISL62771HRTZ-GP-U		
INPUTS		OUTPUTS
DCBATOUT		VGA_CORE
1D5V_VGA_S0		86
Y8288RAC-GP		
INPUTS		OUTPUTS
DCBATOUT		1D5V_VGA_S0

SSID = CPU

13	M_B_DQ00	13	M_B_CLK0
13	M_B_DQ01	13	M_B_CLK#0
13	M_B_DQ02	13	M_B_CLK1
13	M_B_DQ03	13	M_B_CLK#1
13	M_B_DQ04		
13	M_B_DQ05		
13	M_B_DQ06	13	M_B_CKE0
13	M_B_DQ07	13	M_B_CKE1
13	M_B_DQ08		
13	M_B_DQ09	13	M_B_CS#0
13	M_B_DQ10	13	M_B_CS#1
13	M_B_DQ11		
13	M_B_DQ12	13	M_B_ODT0
13	M_B_DQ13	13	M_B_ODT1
13	M_B_DQ14		
13	M_B_DQ15	13	M_B_A16
13	M_B_DQ16	13	M_B_A14
13	M_B_DQ17	13	M_B_A15
13	M_B_DQ18		
13	M_B_DQ19		
13	M_B_DQ20	13	M_B_BA0
13	M_B_DQ21	13	M_B_BA1
13	M_B_DQ22	13	M_B_BG0
13	M_B_DQ23		
13	M_B_DQ24	13	M_B_A0
13	M_B_DQ25	13	M_B_A1
13	M_B_DQ26	13	M_B_A2
13	M_B_DQ27	13	M_B_A3
13	M_B_DQ28	13	M_B_A4
13	M_B_DQ29	13	M_B_A5
13	M_B_DQ30	13	M_B_A6
13	M_B_DQ31	13	M_B_A7
13	M_B_DQ32	13	M_B_A8
13	M_B_DQ33	13	M_B_A9
13	M_B_DQ34	13	M_B_A10
13	M_B_DQ35	13	M_B_A11
13	M_B_DQ36	13	M_B_A12
13	M_B_DQ37	13	M_B_A13
13	M_B_DQ38	13	M_B_BG1
13	M_B_DQ39	13	M_B_ACT_N
13	M_B_DQ40		
13	M_B_DQ41	13	M_B_PARITY
13	M_B_DQ42	13	M_B_ALERT_N
13	M_B_DQ43		
13	M_B_DQ44	13	M_B_DQS_DN0
13	M_B_DQ45	13	M_B_DQS_DN1
13	M_B_DQ46	13	M_B_DQS_DN2
13	M_B_DQ47	13	M_B_DQS_DN3
13	M_B_DQ48	13	M_B_DQS_DN4
13	M_B_DQ49	13	M_B_DQS_DN5
13	M_B_DQ50	13	M_B_DQS_DN6
13	M_B_DQ51	13	M_B_DQS_DN7
13	M_B_DQ52		
13	M_B_DQ53	13	M_B_DQS_DP0
13	M_B_DQ54	13	M_B_DQS_DP1
13	M_B_DQ55	13	M_B_DQS_DP2
13	M_B_DQ56	13	M_B_DQS_DP3
13	M_B_DQ57	13	M_B_DQS_DP4
13	M_B_DQ58	13	M_B_DQS_DP5
13	M_B_DQ59	13	M_B_DQS_DP6
13	M_B_DQ60	13	M_B_DQS_DP7
13	M_B_DQ61		
13	M_B_DQ62		
13	M_B_DQ63		

12 V_SM_VREF_CNTA
13 V_SM_VREF_CNTB



CPU1B 2 OF 13

M_B_DQ00	BT11	DDR1_DQ_0/DDR0_DQ_16	DDR1_CKP_0/DDR1_CKP_0	AM9	M_B_CLK0
M_B_DQ01	BR11	DDR1_DQ_1/DDR0_DQ_17	DDR1_CKN_0/DDR1_CKN_0	AN9	M_B_CLK#0
M_B_DQ02	BT9	DDR1_DQ_2/DDR0_DQ_18	DDR1_CKP_1/DDR1_CKP_1	AM7	M_B_CLK1
M_B_DQ03	BR8	DDR1_DQ_3/DDR0_DQ_19	DDR1_CKN_1/DDR1_CKN_1	AM8	M_B_CLK#1
M_B_DQ04	BP11	DDR1_DQ_4/DDR0_DQ_20	NC/DDR1_CKP_2	AM11	
M_B_DQ05	BN11	DDR1_DQ_5/DDR0_DQ_21	NC/DDR1_CKN_2	AM10	
M_B_DQ06	BP8	DDR1_DQ_6/DDR0_DQ_22	NC/DDR1_CKP_3	AJ10	
M_B_DQ07	BN8	DDR1_DQ_7/DDR0_DQ_23	NC/DDR1_CKN_3	AJ11	
M_B_DQ08	BL12	DDR1_DQ_8/DDR0_DQ_24			
M_B_DQ09	BL11	DDR1_DQ_9/DDR0_DQ_25	DDR1_CKE_0/DDR1_CKE_0	AT8	M_B_CKE0
M_B_DQ10	BL8	DDR1_DQ_10/DDR0_DQ_26	DDR1_CKE_1/DDR1_CKE_1	AT10	M_B_CKE1
M_B_DQ11	BJ8	DDR1_DQ_11/DDR0_DQ_27	DDR1_CKE_2/DDR1_CKE_2	AT7	
M_B_DQ12	BJ11	DDR1_DQ_12/DDR0_DQ_28	DDR1_CKE_3/DDR1_CKE_3	AT11	
M_B_DQ13	BL7	DDR1_DQ_13/DDR0_DQ_29			
M_B_DQ14	BL7	DDR1_DQ_14/DDR0_DQ_30	DDR1_CS#_0/DDR1_CS#_0	AF11	M_B_CS#0
M_B_DQ15	BJ7	DDR1_DQ_15/DDR0_DQ_31	DDR1_CS#_1/DDR1_CS#_1	AE7	M_B_CS#1
M_B_DQ16	BG11	DDR1_DQ_16/DDR0_DQ_48	NC/DDR1_CS#_2	AF10	
M_B_DQ17	BG10	DDR1_DQ_17/DDR0_DQ_49	NC/DDR1_CS#_3	AE10	
M_B_DQ18	BG8	DDR1_DQ_18/DDR0_DQ_50			
M_B_DQ19	BF8	DDR1_DQ_19/DDR0_DQ_51	DDR1_ODT_0/DDR1_ODT_0	AF7	M_B_ODT0
M_B_DQ20	BF11	DDR1_DQ_20/DDR0_DQ_52	NC/DDR1_ODT_1	AE8	M_B_ODT1
M_B_DQ21	BF10	DDR1_DQ_21/DDR0_DQ_53	NC/DDR1_ODT_2	AE9	
M_B_DQ22	BG7	DDR1_DQ_22/DDR0_DQ_54	NC/DDR1_ODT_3	AE1	
M_B_DQ23	BF7	DDR1_DQ_23/DDR0_DQ_55			
M_B_DQ24	BB11	DDR1_DQ_24/DDR0_DQ_56	DDR1_CAB_3/DDR1_MA_16	AH10	M_B_A16
M_B_DQ25	BC11	DDR1_DQ_25/DDR0_DQ_57	DDR1_CAB_2/DDR1_MA_14	AH11	M_B_A14
M_B_DQ26	BB8	DDR1_DQ_26/DDR0_DQ_58	DDR1_CAB_1/DDR1_MA_15	AF8	M_B_A15
M_B_DQ27	BC8	DDR1_DQ_27/DDR0_DQ_59			
M_B_DQ28	BC10	DDR1_DQ_28/DDR0_DQ_60	DDR1_CAB_4/DDR1_BA_0	AH8	M_B_BA0
M_B_DQ29	BB10	DDR1_DQ_29/DDR0_DQ_61	DDR1_CAB_6/DDR1_BA_1	AH9	M_B_BA1
M_B_DQ30	BC7	DDR1_DQ_30/DDR0_DQ_62	DDR1_CAA_5/DDR1_BG_0	AR9	M_B_BG0
M_B_DQ31	BB7	DDR1_DQ_31/DDR0_DQ_63			
M_B_DQ32	AA11	DDR1_DQ_32/DDR1_DQ_16	DDR1_CAB_9/DDR1_MA_0	AJ9	M_B_A0
M_B_DQ33	AA10	DDR1_DQ_33/DDR1_DQ_17	DDR1_CAB_8/DDR1_MA_1	AK6	M_B_A1
M_B_DQ34	AC11	DDR1_DQ_34/DDR1_DQ_18	DDR1_CAB_5/DDR1_MA_2	AK5	M_B_A2
M_B_DQ35	AC10	DDR1_DQ_35/DDR1_DQ_19	NC/DDR1_MA_3	AL5	M_B_A3
M_B_DQ36	AA7	DDR1_DQ_36/DDR1_DQ_20	NC/DDR1_MA_4	AL6	M_B_A4
M_B_DQ37	AA8	DDR1_DQ_37/DDR1_DQ_21	DDR1_CAA_0/DDR1_MA_5	AN7	M_B_A6
M_B_DQ38	AC8	DDR1_DQ_38/DDR1_DQ_22	DDR1_CAA_2/DDR1_MA_6	AN10	M_B_A7
M_B_DQ39	AC7	DDR1_DQ_39/DDR1_DQ_23	DDR1_CAA_4/DDR1_MA_7		
M_B_DQ40	W8	DDR1_DQ_40/DDR1_DQ_24	DDR1_CAA_3/DDR1_MA_8	AN8	M_B_A8
M_B_DQ41	W7	DDR1_DQ_41/DDR1_DQ_25	DDR1_CAA_1/DDR1_MA_9	AR11	M_B_A9
M_B_DQ42	V10	DDR1_DQ_42/DDR1_DQ_26	DDR1_CAB_7/DDR1_MA_10	AH7	M_B_A10
M_B_DQ43	V11	DDR1_DQ_43/DDR1_DQ_27	DDR1_CAB_6/DDR1_MA_11	AN11	M_B_A11
M_B_DQ44	W11	DDR1_DQ_44/DDR1_DQ_28	DDR1_CAA_7/DDR1_MA_11	AR10	M_B_A12
M_B_DQ45	W10	DDR1_DQ_45/DDR1_DQ_29	DDR1_CAB_9/DDR1_MA_12	AF9	M_B_A13
M_B_DQ46	V7	DDR1_DQ_46/DDR1_DQ_30	DDR1_CAB_8/DDR1_MA_13	AR7	M_B_BG1
M_B_DQ47	V8	DDR1_DQ_47/DDR1_DQ_31	DDR1_CAA_9/DDR1_BG_1	AT9	M_B_ACT_N
M_B_DQ48	R11	DDR1_DQ_48/DDR1_DQ_48	DDR1_CAA_8/DDR1_ACT#		
M_B_DQ49	P11	DDR1_DQ_49/DDR1_DQ_49	NC/DDR1_PAR	AJ7	M_B_PARITY
M_B_DQ50	P7	DDR1_DQ_50/DDR1_DQ_50	NC/DDR1_ALERT#	AR8	M_B_ALERT_N
M_B_DQ51	R8	DDR1_DQ_51/DDR1_DQ_51			
M_B_DQ52	R10	DDR1_DQ_52/DDR1_DQ_52			
M_B_DQ53	P10	DDR1_DQ_53/DDR1_DQ_53	DDR1_DQSN_0/DDR0_DQSN_2	BN9	M_B_DQS_DN0
M_B_DQ54	R7	DDR1_DQ_54/DDR1_DQ_54	DDR1_DQSN_1/DDR0_DQSN_3	BL9	M_B_DQS_DN1
M_B_DQ55	P8	DDR1_DQ_55/DDR1_DQ_55	DDR1_DQSN_2/DDR0_DQSN_6	BG9	M_B_DQS_DN2
M_B_DQ56	L11	DDR1_DQ_56/DDR1_DQ_56	DDR1_DQSN_3/DDR0_DQSN_7	BC9	M_B_DQS_DN3
M_B_DQ57	M11	DDR1_DQ_57/DDR1_DQ_57	DDR1_DQSN_4/DDR1_DQSN_2	AC9	M_B_DQS_DN4
M_B_DQ58	L7	DDR1_DQ_58/DDR1_DQ_58	DDR1_DQSN_5/DDR1_DQSN_3	W9	M_B_DQS_DN5
M_B_DQ59	M8	DDR1_DQ_59/DDR1_DQ_59	DDR1_DQSN_6/DDR1_DQSN_6	R9	M_B_DQS_DN6
M_B_DQ60	L10	DDR1_DQ_60/DDR1_DQ_60	DDR1_DQSN_7/DDR1_DQSN_7	M9	M_B_DQS_DN7
M_B_DQ61	M10	DDR1_DQ_61/DDR1_DQ_61			
M_B_DQ62	M7	DDR1_DQ_62/DDR1_DQ_62	DDR1_DQSP_0/DDR0_DQSP_2	BP9	M_B_DQS_DP0
M_B_DQ63	L8	DDR1_DQ_63/DDR1_DQ_63	DDR1_DQSP_1/DDR0_DQSP_3	BJ9	M_B_DQS_DP1
AW11	NC/DDR1_ECC_0		DDR1_DQSP_2/DDR0_DQSP_6	BF9	M_B_DQS_DP2
AY11	NC/DDR1_ECC_1		DDR1_DQSP_3/DDR0_DQSP_7	BB9	M_B_DQS_DP3
AW8	NC/DDR1_ECC_2		DDR1_DQSP_4/DDR1_DQSP_2	AA9	M_B_DQS_DP4
AY10	NC/DDR1_ECC_3		DDR1_DQSP_5/DDR1_DQSP_3	V9	M_B_DQS_DP5
AW10	NC/DDR1_ECC_4		DDR1_DQSP_6/DDR1_DQSP_6	P9	M_B_DQS_DP6
AY7	NC/DDR1_ECC_5		DDR1_DQSP_7/DDR1_DQSP_7	L9	M_B_DQS_DP7
AW7	NC/DDR1_ECC_6				
AW9	NC/DDR1_ECC_7		DDR1_DQSP_8/DDR1_DQSP_8	AW9	

Selek CMLH N18E

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title CPU_DDR_CHB			
Size A3	Document Number Selek CML-H	Rev A00	
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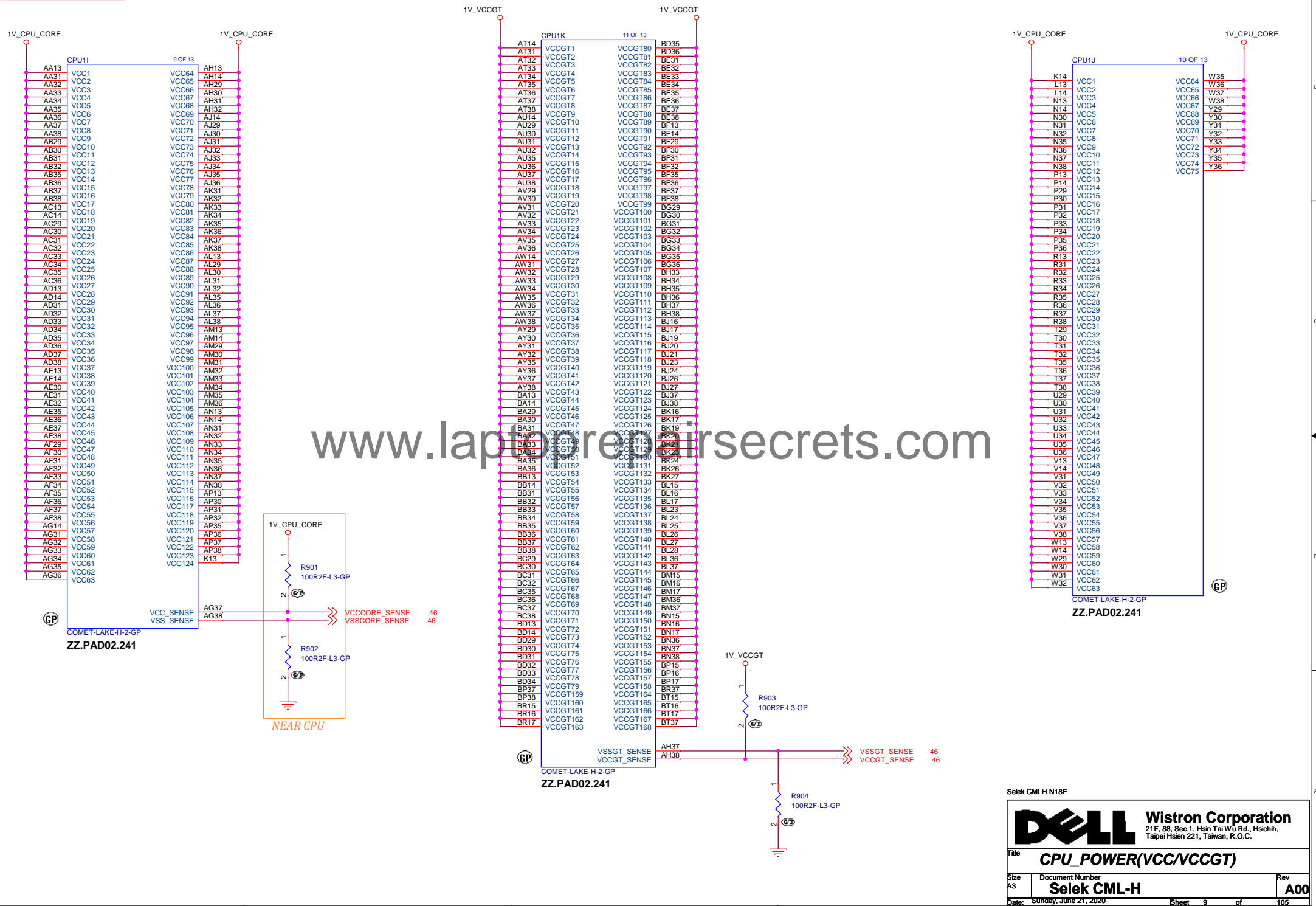
**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title**CPU_GND**

SizeA3Document Number**Selek CML-H**Rev**A00**

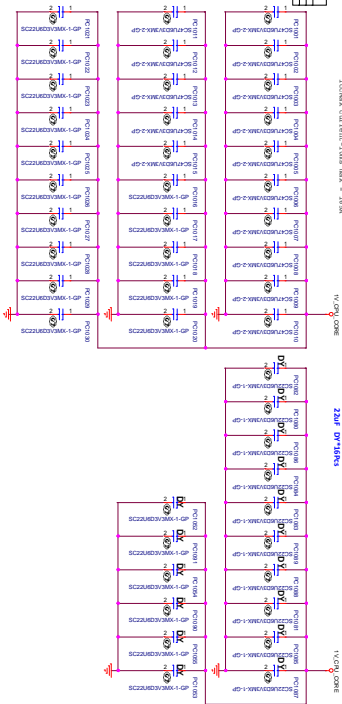
Date: Sunday, June 21, 2020Sheet7of105

SSID = CPU

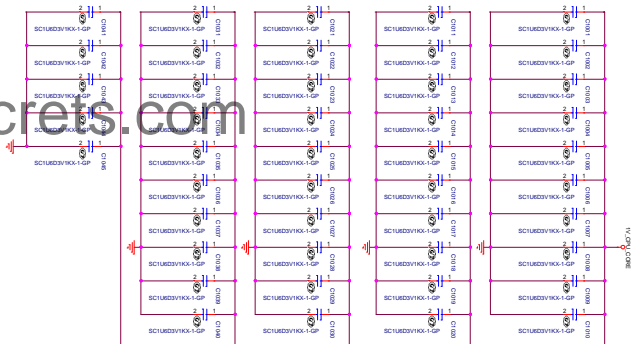


IC: 1.20A @ 45W
IC: 1.20A @ 45W
IC: 1.20A @ 45W

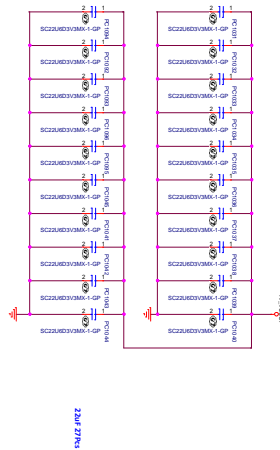
IC	Value	Unit
IC1	1.20A	A
IC2	1.20A	A
IC3	1.20A	A



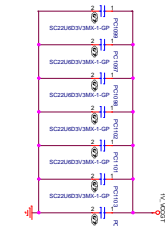
1uF 63V



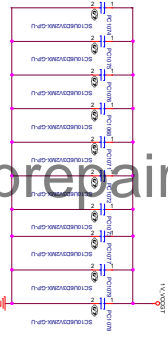
IC: 1.20A @ 45W
IC: 1.20A @ 45W
IC: 1.20A @ 45W



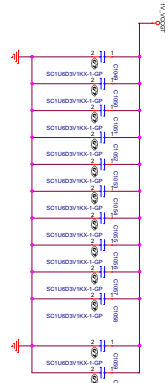
22uF 50V



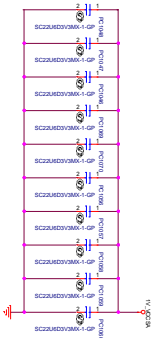
22uF 50V



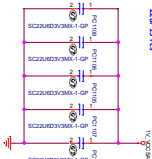
1uF 22V



IC: 1.20A @ 45W
IC: 1.20A @ 45W
IC: 1.20A @ 45W



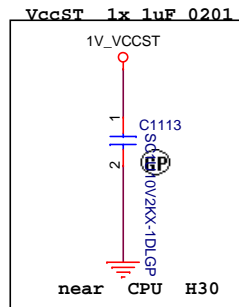
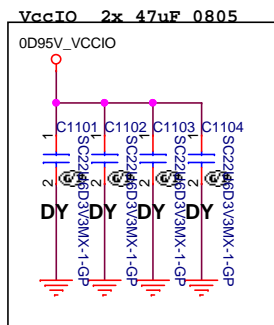
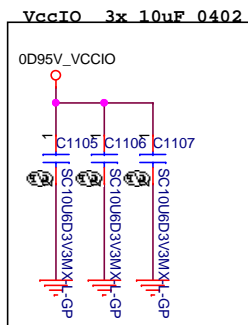
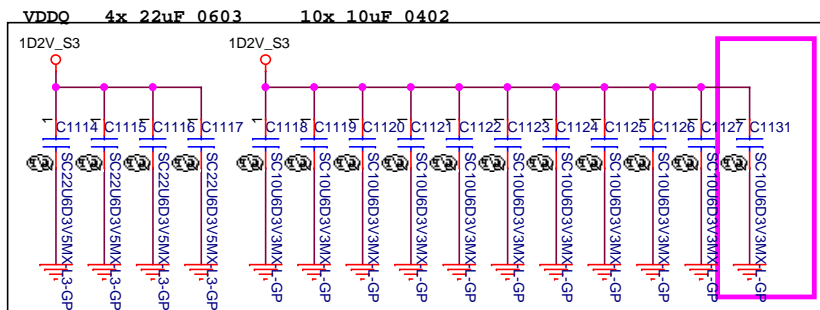
22uF 50V



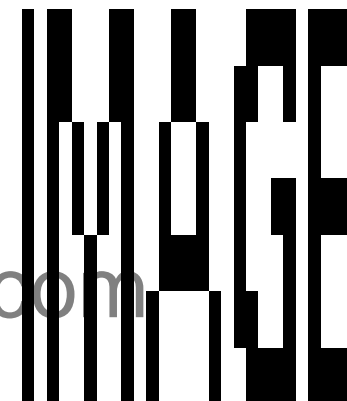
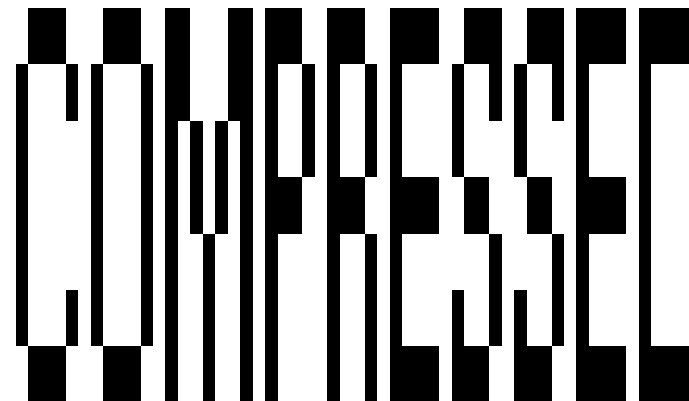
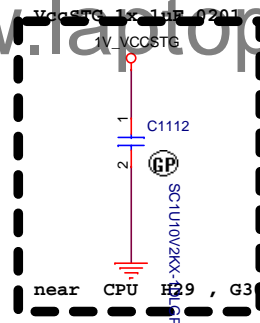
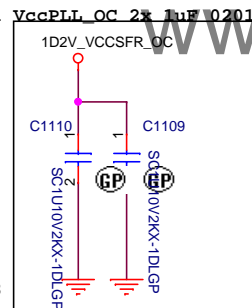
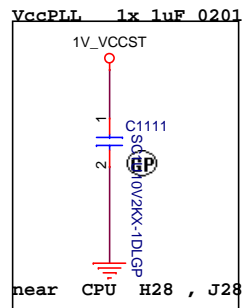
22uF 50V



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VR: +/-5% or +/-50mV
Place close to VR output



Selek CMLH N18E

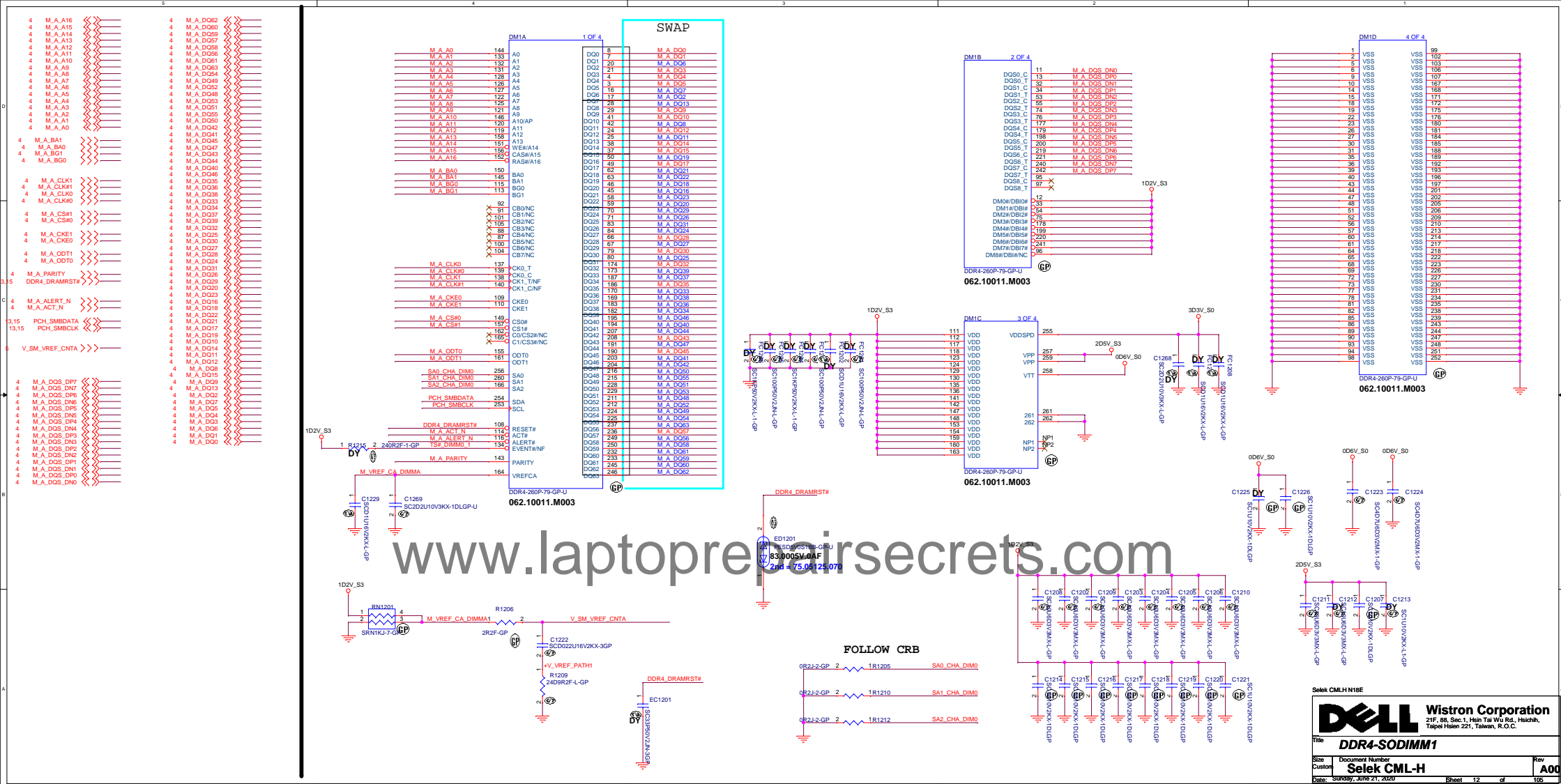


Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title
CPU (Power CAP2)

Size	Document Number	Rev
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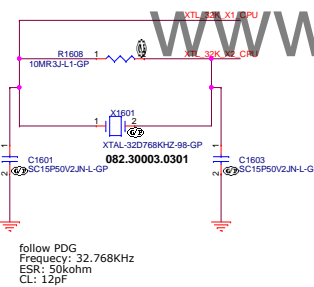
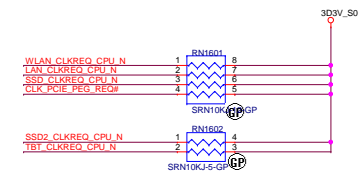
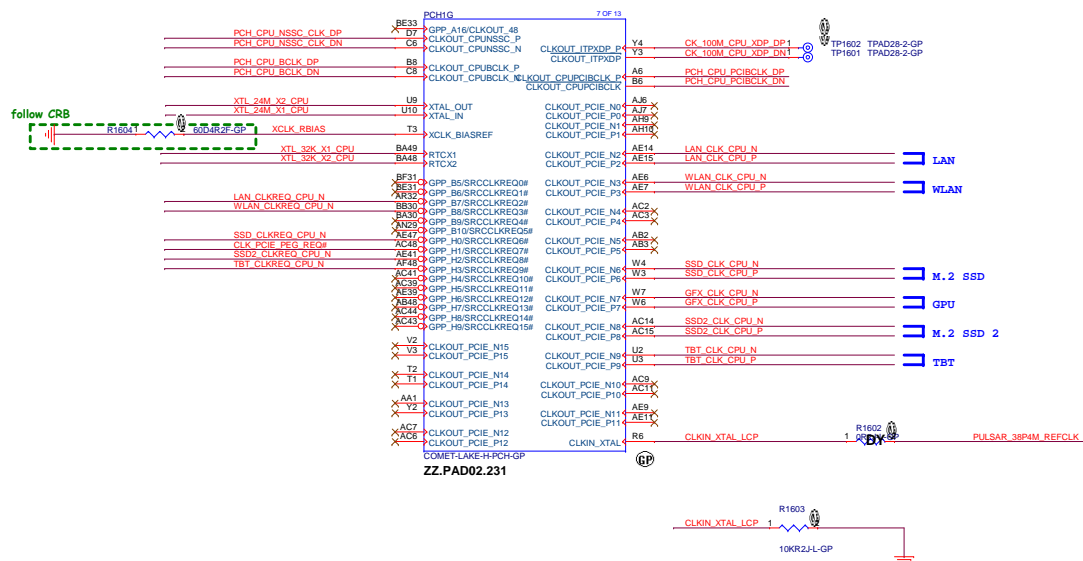
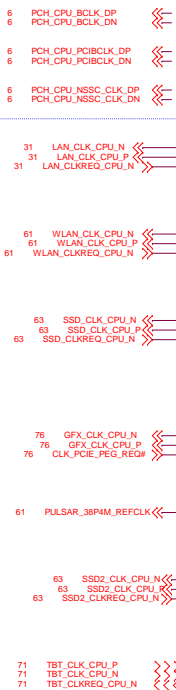


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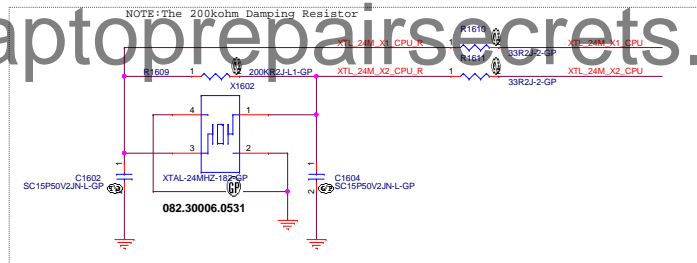
Selek CMLH N18E

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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TO CPU CLOCK



follow PDG
Frequency: 32.768KHz
ESR: 50kohm
CL: 12pF

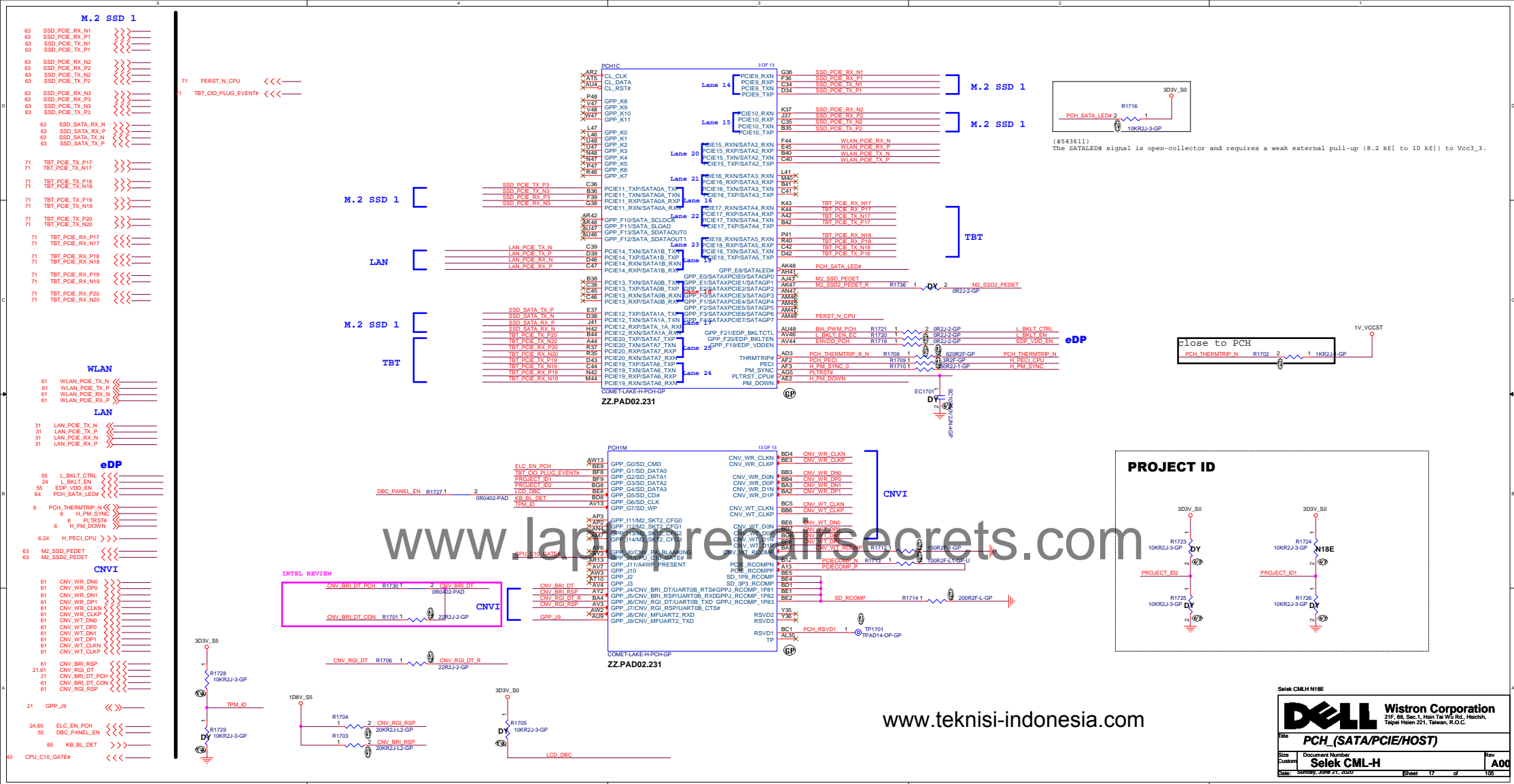


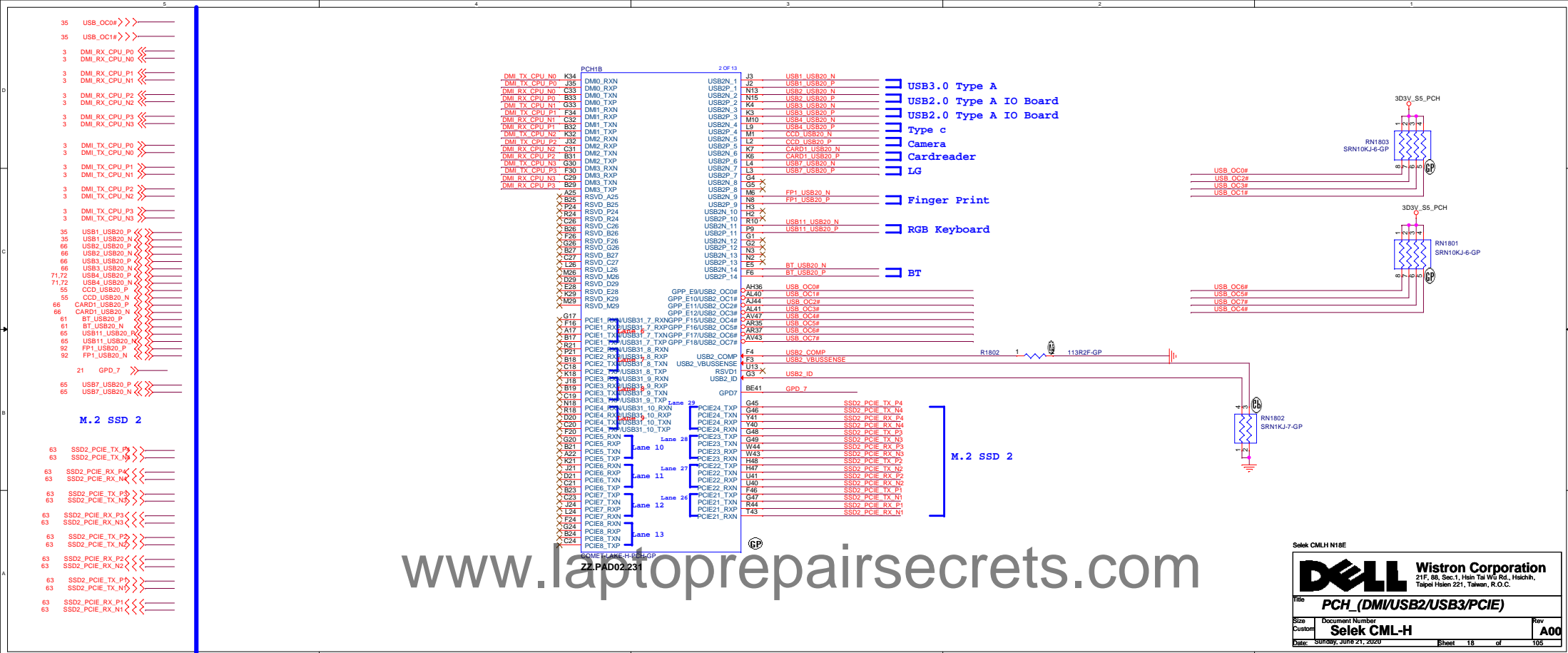
follow PDG
Frequency: 24MHz
Series Resistance: 1-2-30ohm-MAX
CL: 12pF

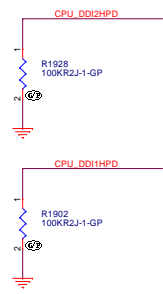
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Selek CMLH N18E

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.			
Title	PCH (CLK)		
Size	Document Number	Rev	
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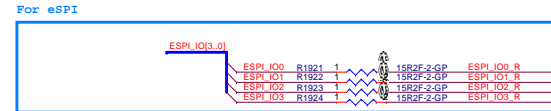
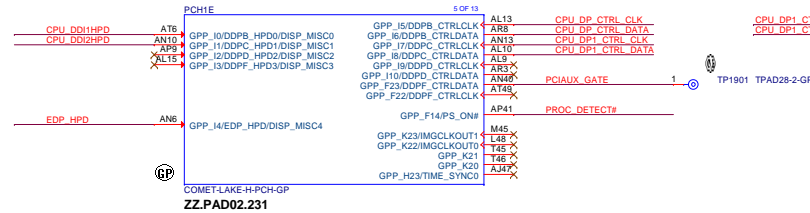




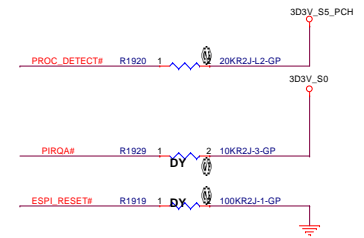
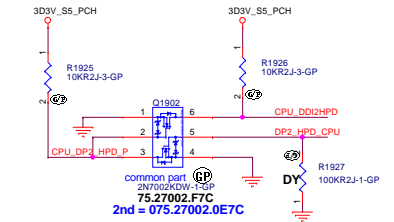
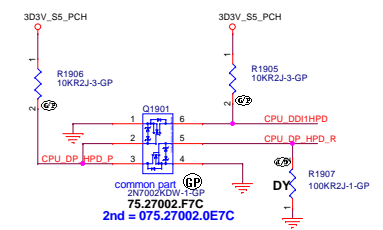
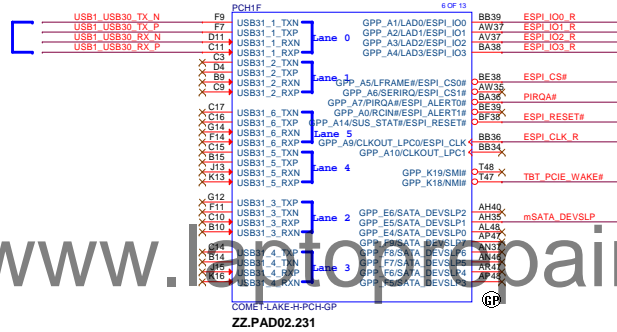
6.3.3 Embedded DisplayPort* Hot-Plug Detect Implementation

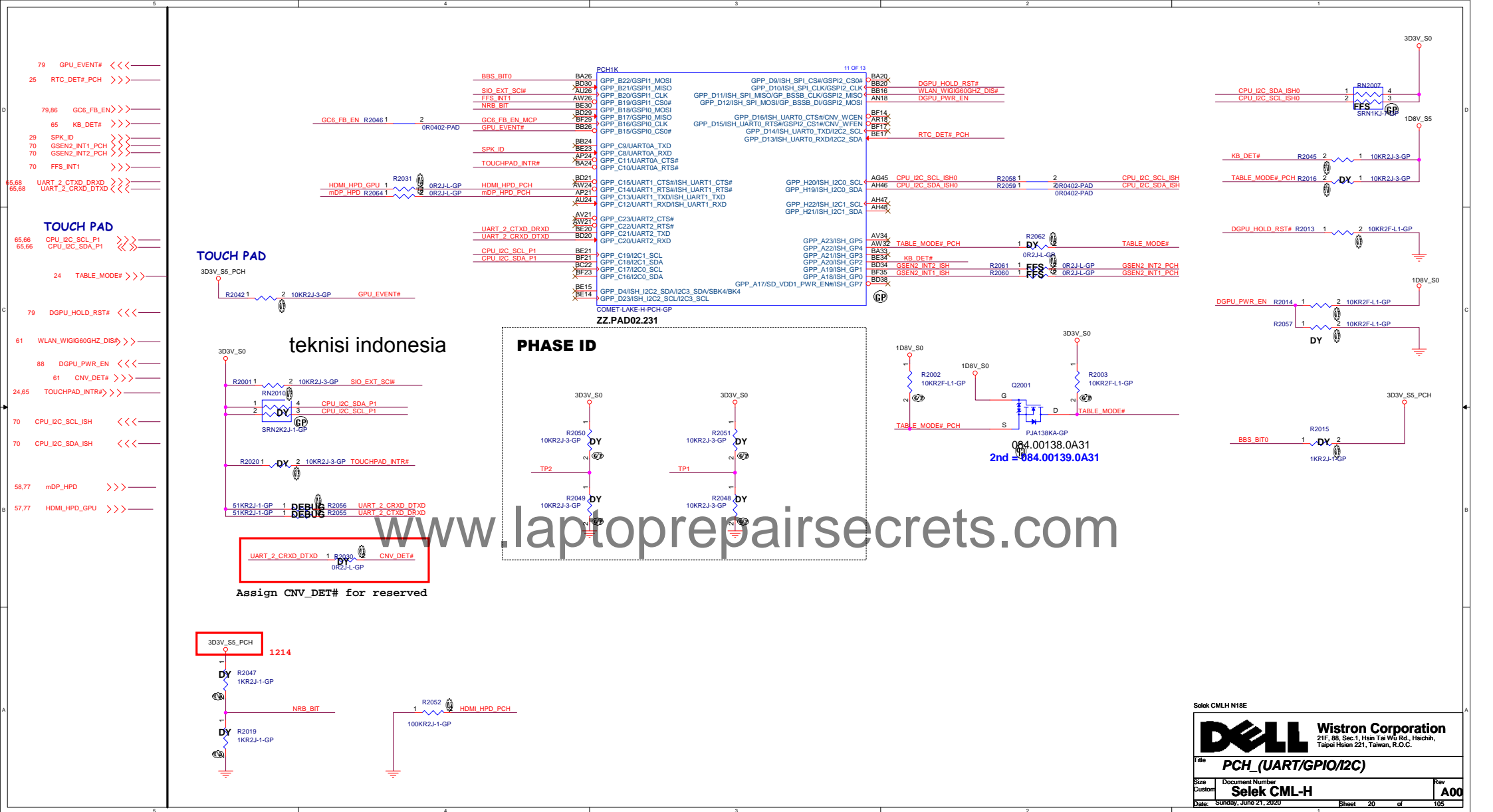
Hot-plug detect (HPD) is an output from eDP* sink device and it is a active high signal.

Note: When using eDP bifurcation for DP-VGA Topology, need to use HPD for DDIE (DDPE_HPDP) for HPD connectivity.



USB3.0 Type A



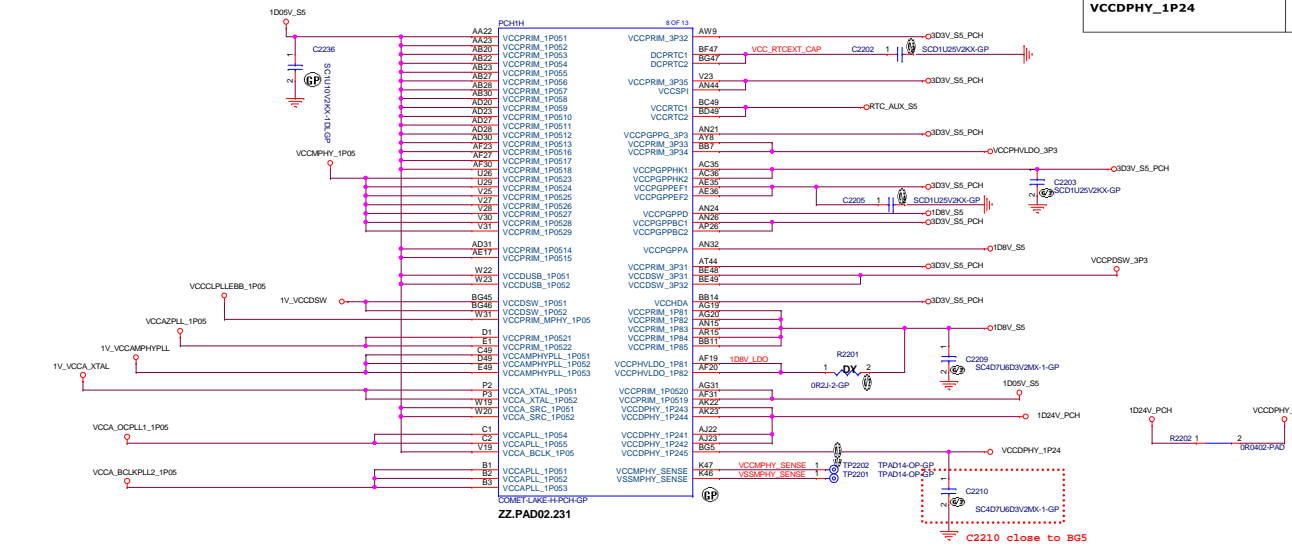


GPIO	GPP_B14 SPKR	GPP_B18 GSPIO_MOSI	GPP_C2 SMBALERT#	GPP_B22 GSPII_MOSI	GPP_C5 SMBALERT#	SPI0_MOSI SPI0_MISO	GPP_H15 SML3ALERT#
Schematic		default is internal pull down add TP at PCH side		default is internal pull down add TP at PCH side			

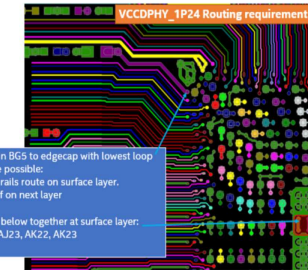
GPIO	GPP_B23 SML1ALERT# PCHHOT#	SPI0_IO2	SPI0_IO3	HDA_SDO I2S0_TXD	GPP_H12 SML2ALERT#	GPP_I6 DDPB_CTRLDATA	GPP_I8 DDPC_CTRLDATA
Schematic					GPP_H12 add TP at PCH side	DDPB_CTRLDATA PU at Page.19	weak internal Pull-down.

GPIO	GPP_I10 DDPD_CTRLDATA	GPP_F23 DPPF_CTRLDATA	GPP_J4 CNV_BRI_DT UART0_RTS#	GPP_J6 CNV_RGI_DT UART0_TXD	GPP_I9 GPD7
Schematic	weak internal Pull-down.	weak internal pull-down.			

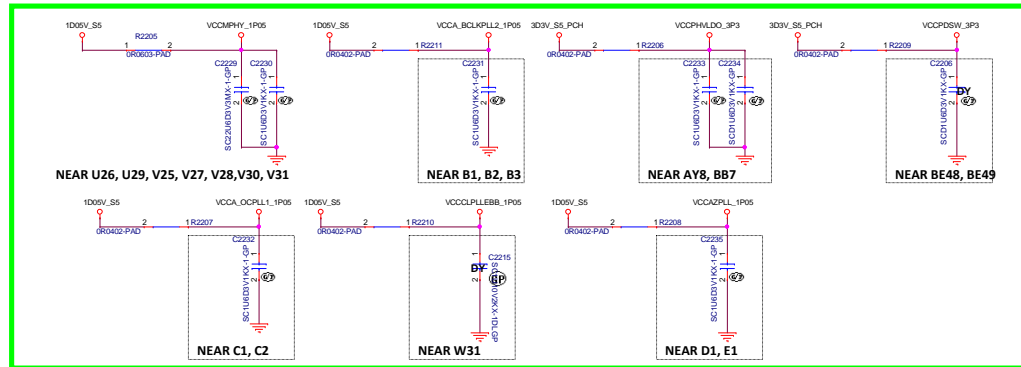
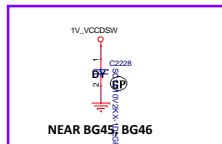
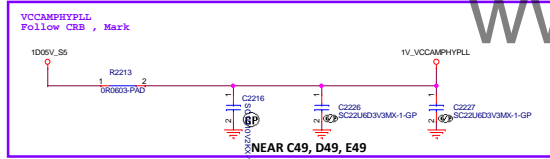
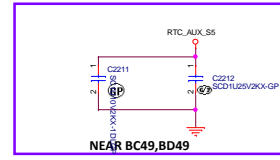
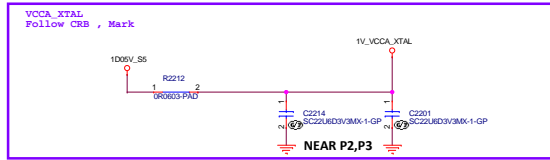
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IMAGE

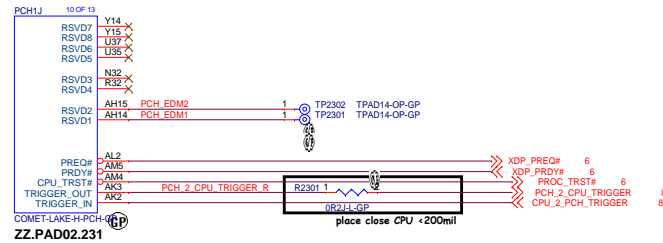
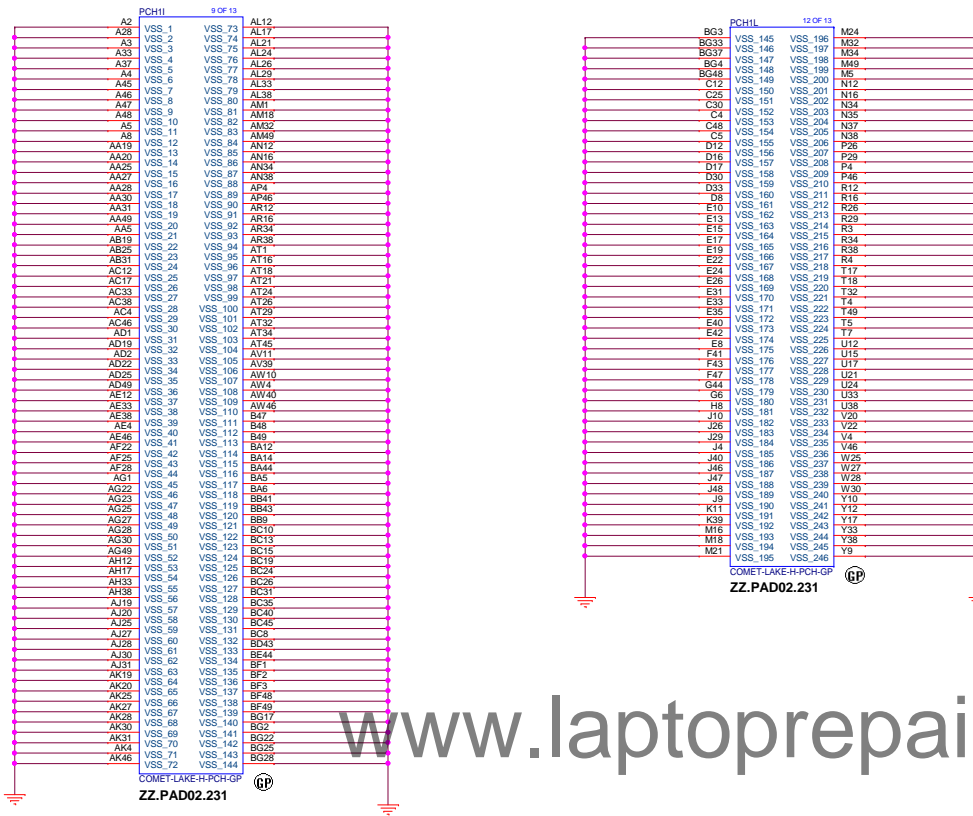


CFL PCH-H VCCDPHY_1P24 Routing



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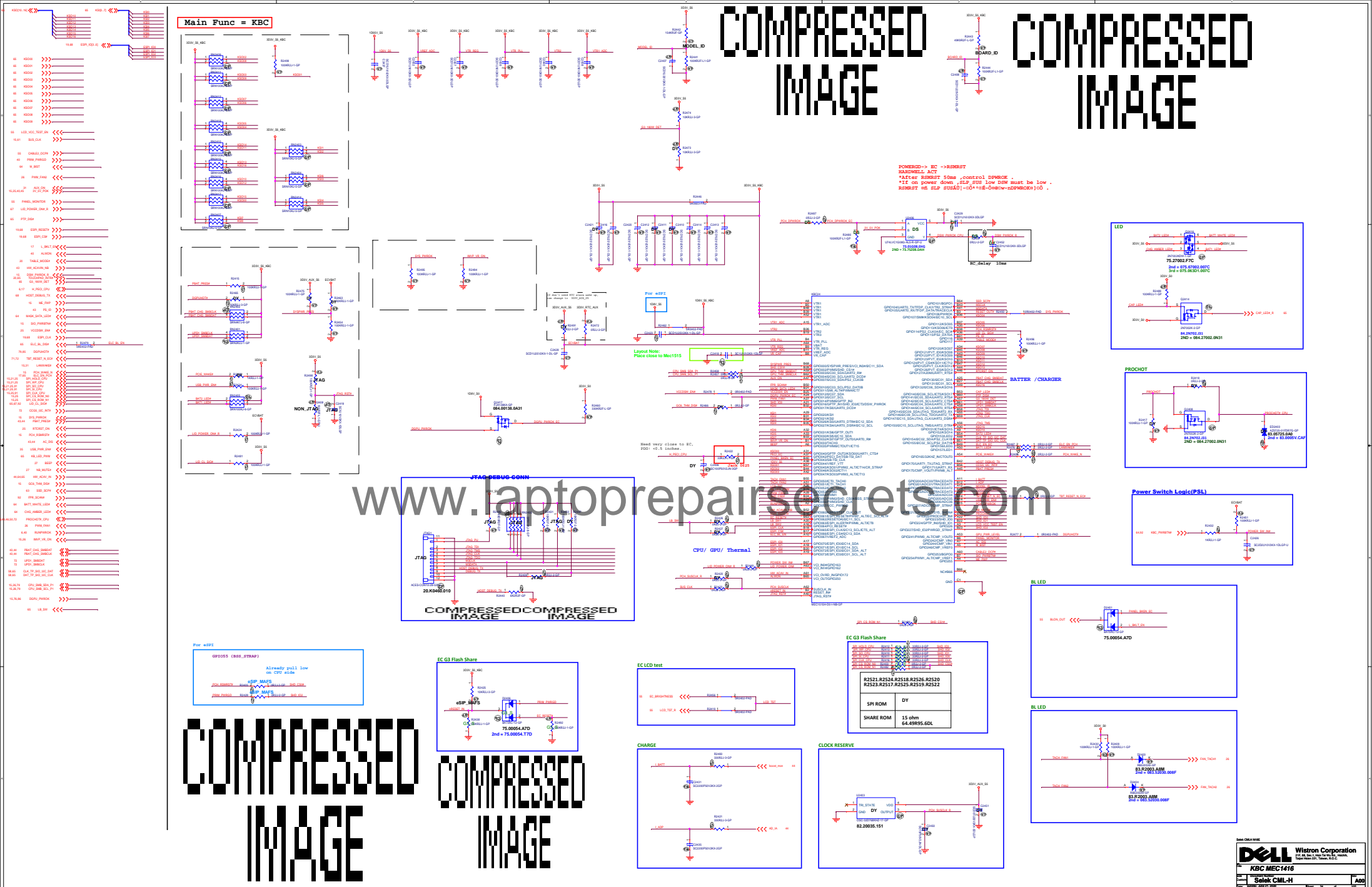




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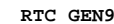
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.			
Title PCH_(VSS/GPIO)			
Size	Document Number	Rev	
Custom	Selek CML-H	A00	
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IMAGE




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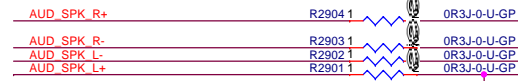
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RESERVED			
Size A4	Document Number Selek CML-H		Rev A00
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Main Func = Audio

27 AUD_SPK_L+ >>>
27 AUD_SPK_L- >>>
27 AUD_SPK_R+ >>>
27 AUD_SPK_R- >>>

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



27 MIC2_VREFO_R >>>
27 MIC2_VREFO_L >>>

27 AUD_RING <<<
27 AUD_HPOUT_L >>>

27 LINE1_L >>>
27 AUD_HPOUT_R >>>

27 LINE1_R >>>
27 AUD_SELEEVE <<<

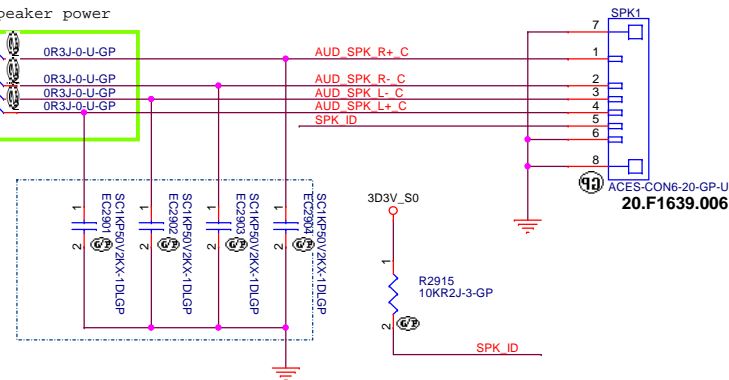
27 AUD_HPJD_N <<<
20 SPK_ID <<<

66 RING2_R >>>
66 AUD_HP1_JACK_L1 >>>

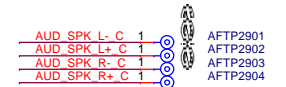
66 JACK_PLUG >>>
66 AUD_HP1_JACK_R1 >>>

66 SLEEVE_R >>>

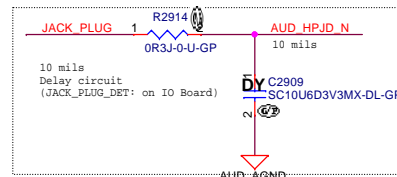
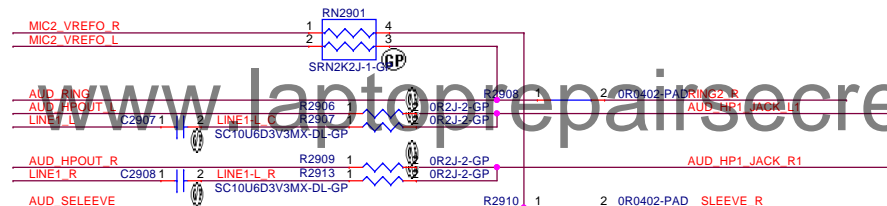
Speaker



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND



Universal Jack (Moved to I/O Board)




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DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

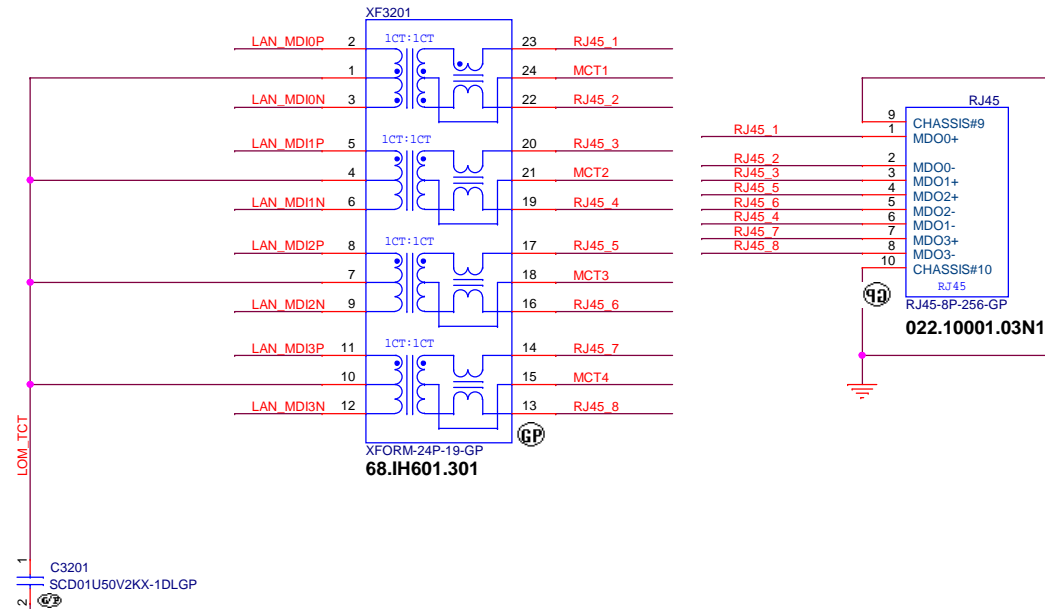
Title Audio IO		
Size A3	Document Number Selek CML-H	Rev A00
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Sheet 29 of 105		

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Selek CMLH N18E

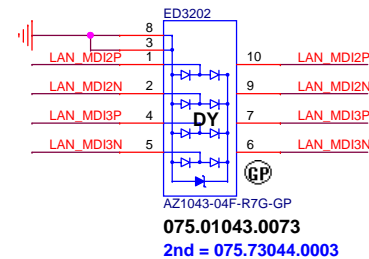
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A	Document Number Selek CML-H		Rev A00
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SSID = LAN



Follow Reference Schematic 0.01uF-0.4uF

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SSID = Card Reader


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Selek CMLH W18E

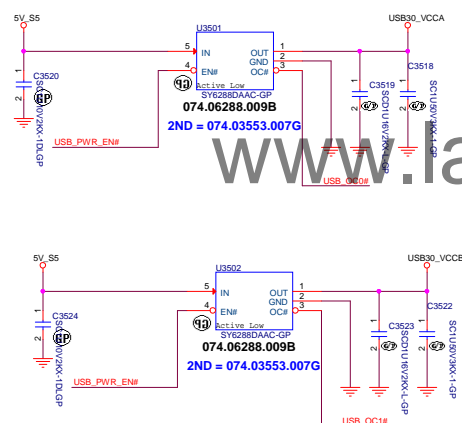
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A2	Document Number Selek CML-H		Rev A00
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Title (Reserved)			
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USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+




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TitleCharger

Size
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Document Number
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A00

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Title (Reserved)			
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SSID = USB3.0 Redriver


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		Wistron Corporation 21F, 88, Sec. 1, Minsheng Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		USB 3.0 Redriver	
Size	Document Number	Rev	
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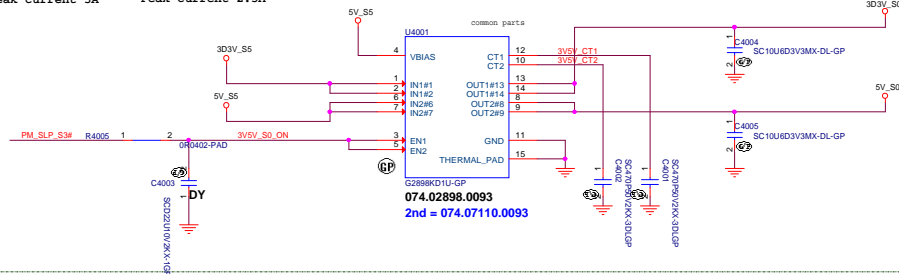
Selek CMLH N18E

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A	Document Number Selek CML-H		Rev A00
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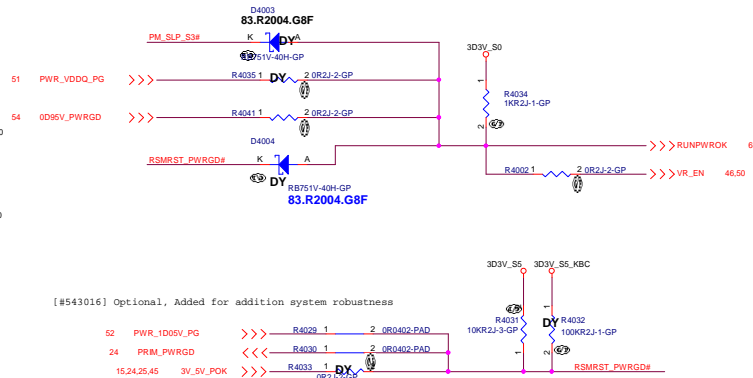
Power Sequence

5V_S0 **3D3V_S0**
5V_S0 Consumption
Peak current 5A
3D3V_S0 Consumption
Peak current 2.5A

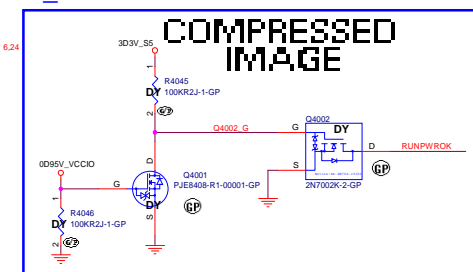
ROSA Run Power



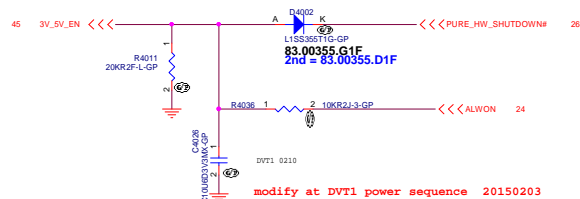
Power Good



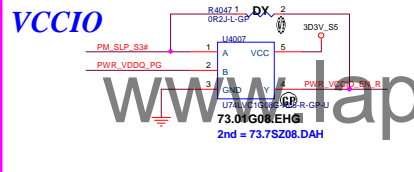
V_TREE



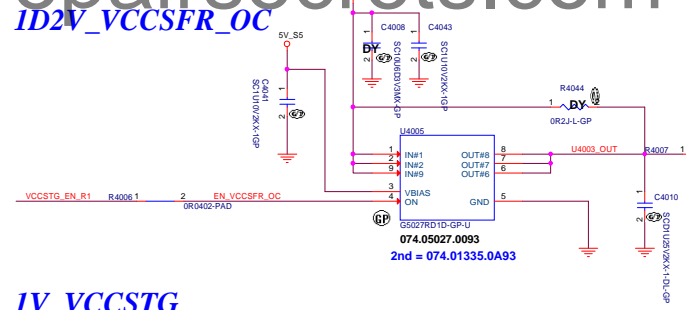
IV_VCCST



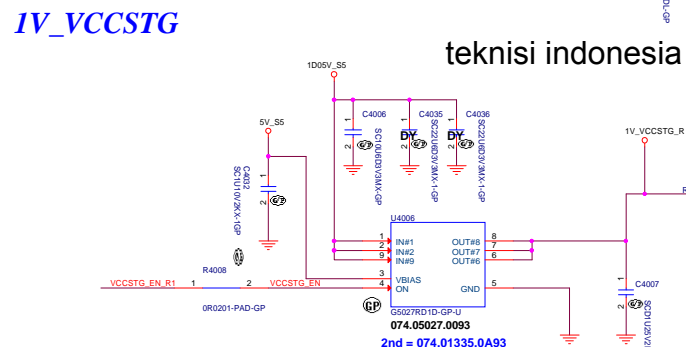
VCCIO



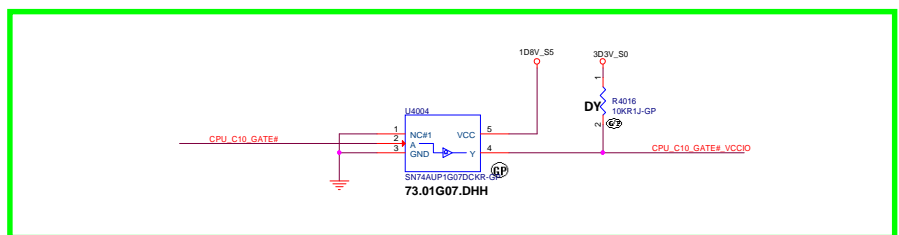
ID2V_VCCSFR_OC



IV_VCCSTG



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Selekt CMLH N18E

Main Func = Power & Sequence

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Title

Connected_Standby(1/2)+DS3

Size

A3

Document Number

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Main Func = M-BAT Input



718

Size

A2

Date: Sunday, June 21, 2020

DCIN

Selek CML-H

Rev	
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A00

Select CMLN WISE			
		Wistron Corporation 10F, 208, Sec. 1, Hsinchu Rd. 1st, Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
The POWER (ISL95522 CHG)			
Case	Document Number		
Customer			
Solek CML-H			
Case	Order Date	44 of	105

The schematic diagram, titled "NCP81266 For CPUCORE", illustrates the power and ground connections for a system. It features a central power management IC (NCP81266) connected to various components. Key components and their connections include:

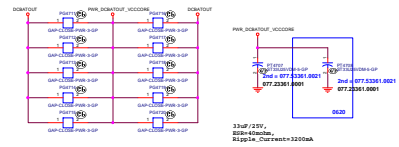
- CPUCORE:** Connected to VCCORE, VCCORE_P, and VCCORE_N.
- GPU:** Connected to VGPU, VGPU_P, and VGPU_N.
- Memory Modules:** Connected to VDD, VDD_P, and VDD_N.
- Other Components:** Includes VCC, VCC_P, VCC_N, VCC2, VCC2_P, VCC2_N, VCC3, VCC3_P, VCC3_N, VCC4, VCC4_P, VCC4_N, VCC5, VCC5_P, VCC5_N, VCC6, VCC6_P, VCC6_N, VCC7, VCC7_P, VCC7_N, VCC8, VCC8_P, VCC8_N, VCC9, VCC9_P, VCC9_N, VCC10, VCC10_P, VCC10_N, VCC11, VCC11_P, VCC11_N, VCC12, VCC12_P, VCC12_N, VCC13, VCC13_P, VCC13_N, VCC14, VCC14_P, VCC14_N, VCC15, VCC15_P, VCC15_N, VCC16, VCC16_P, VCC16_N, VCC17, VCC17_P, VCC17_N, VCC18, VCC18_P, VCC18_N, VCC19, VCC19_P, VCC19_N, VCC20, VCC20_P, VCC20_N, VCC21, VCC21_P, VCC21_N, VCC22, VCC22_P, VCC22_N, VCC23, VCC23_P, VCC23_N, VCC24, VCC24_P, VCC24_N, VCC25, VCC25_P, VCC25_N, VCC26, VCC26_P, VCC26_N, VCC27, VCC27_P, VCC27_N, VCC28, VCC28_P, VCC28_N, VCC29, VCC29_P, VCC29_N, VCC30, VCC30_P, VCC30_N, VCC31, VCC31_P, VCC31_N, VCC32, VCC32_P, VCC32_N, VCC33, VCC33_P, VCC33_N, VCC34, VCC34_P, VCC34_N, VCC35, VCC35_P, VCC35_N, VCC36, VCC36_P, VCC36_N, VCC37, VCC37_P, VCC37_N, VCC38, VCC38_P, VCC38_N, VCC39, VCC39_P, VCC39_N, VCC40, VCC40_P, VCC40_N, VCC41, VCC41_P, VCC41_N, VCC42, VCC42_P, VCC42_N, VCC43, VCC43_P, VCC43_N, VCC44, VCC44_P, VCC44_N, VCC45, VCC45_P, VCC45_N, VCC46, VCC46_P, VCC46_N, VCC47, VCC47_P, VCC47_N, VCC48, VCC48_P, VCC48_N, VCC49, VCC49_P, VCC49_N, VCC50, VCC50_P, VCC50_N, VCC51, VCC51_P, VCC51_N, VCC52, VCC52_P, VCC52_N, VCC53, VCC53_P, VCC53_N, VCC54, VCC54_P, VCC54_N, VCC55, VCC55_P, VCC55_N, VCC56, VCC56_P, VCC56_N, VCC57, VCC57_P, VCC57_N, VCC58, VCC58_P, VCC58_N, VCC59, VCC59_P, VCC59_N, VCC60, VCC60_P, VCC60_N, VCC61, VCC61_P, VCC61_N, VCC62, VCC62_P, VCC62_N, VCC63, VCC63_P, VCC63_N, VCC64, VCC64_P, VCC64_N, VCC65, VCC65_P, VCC65_N, VCC66, VCC66_P, VCC66_N, VCC67, VCC67_P, VCC67_N, VCC68, VCC68_P, VCC68_N, VCC69, VCC69_P, VCC69_N, VCC70, VCC70_P, VCC70_N, VCC71, VCC71_P, VCC71_N, VCC72, VCC72_P, VCC72_N, VCC73, VCC73_P, VCC73_N, VCC74, VCC74_P, VCC74_N, VCC75, VCC75_P, VCC75_N, VCC76, VCC76_P, VCC76_N, VCC77, VCC77_P, VCC77_N, VCC78, VCC78_P, VCC78_N, VCC79, VCC79_P, VCC79_N, VCC80, VCC80_P, VCC80_N, VCC81, VCC81_P, VCC81_N, VCC82, VCC82_P, VCC82_N, VCC83, VCC83_P, VCC83_N, VCC84, VCC84_P, VCC84_N, VCC85, VCC85_P, VCC85_N, VCC86, VCC86_P, VCC86_N, VCC87, VCC87_P, VCC87_N, VCC88, VCC88_P, VCC88_N, VCC89, VCC89_P, VCC89_N, VCC90, VCC90_P, VCC90_N, VCC91, VCC91_P, VCC91_N, VCC92, VCC92_P, VCC92_N, VCC93, VCC93_P, VCC93_N, VCC94, VCC94_P, VCC94_N, VCC95, VCC95_P, VCC95_N, VCC96, VCC96_P, VCC96_N, VCC97, VCC97_P, VCC97_N, VCC98, VCC98_P, VCC98_N, VCC99, VCC99_P, VCC99_N, VCC100, VCC100_P, VCC100_N.

The diagram also includes a table of component values and a list of component footprints.

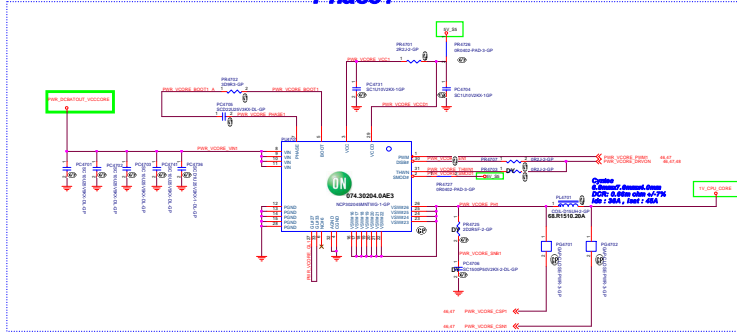
 Wistron Corporation 137-88, Sec. 1, Shuei-Tai Rd., Hsuehshui, Taipei 107, Taiwan, R.O.C.	
POWER (NCP81266, VCORE)	
Case: Soletek CML-H	Part: A00

NCP302045 For VCORE

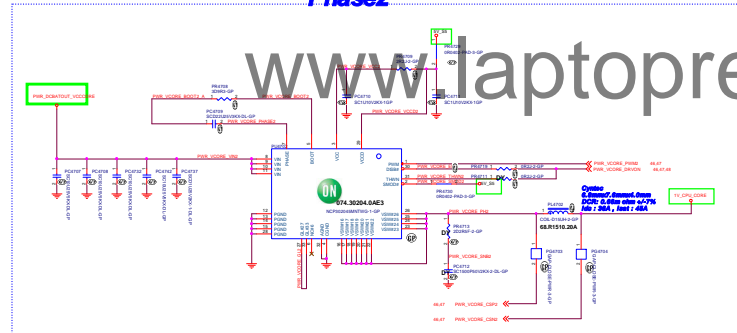
OFFPAGE



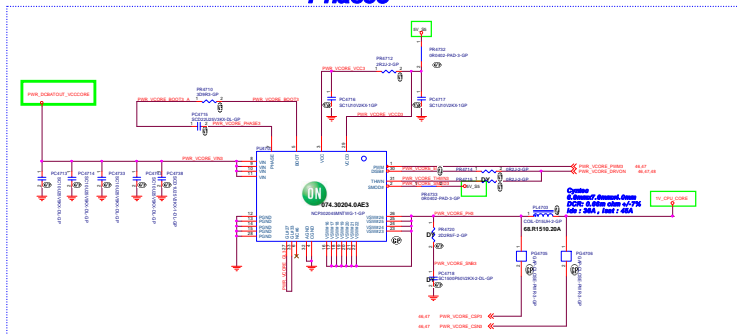
Phase1



Phase2



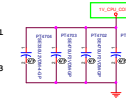
Phase3



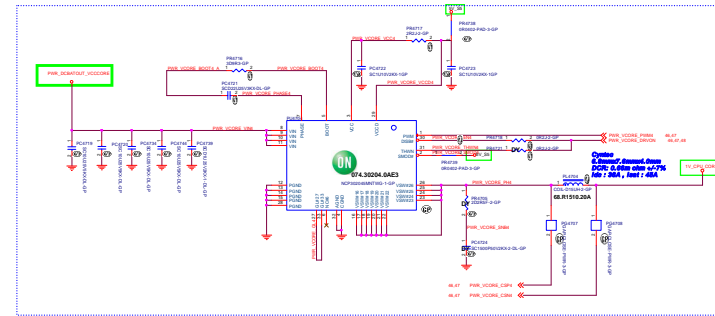
CML H82
Baseline
TDC=140A
Iccmax=86A

CML H82
PERF
TDC=125A
Iccmax=165A

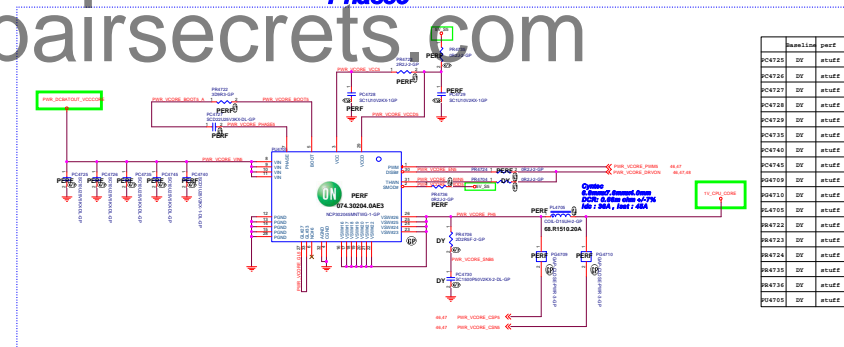
Buck Cap 330uF*1
470uF/25V,
800mA/50mA
Ripple_Curmax=3200mA
Buck Cap 470uF*3
470uF/25V,
800mA/50mA
Ripple_Curmax=3200mA
4.5mm * 7.5mm



Phase4

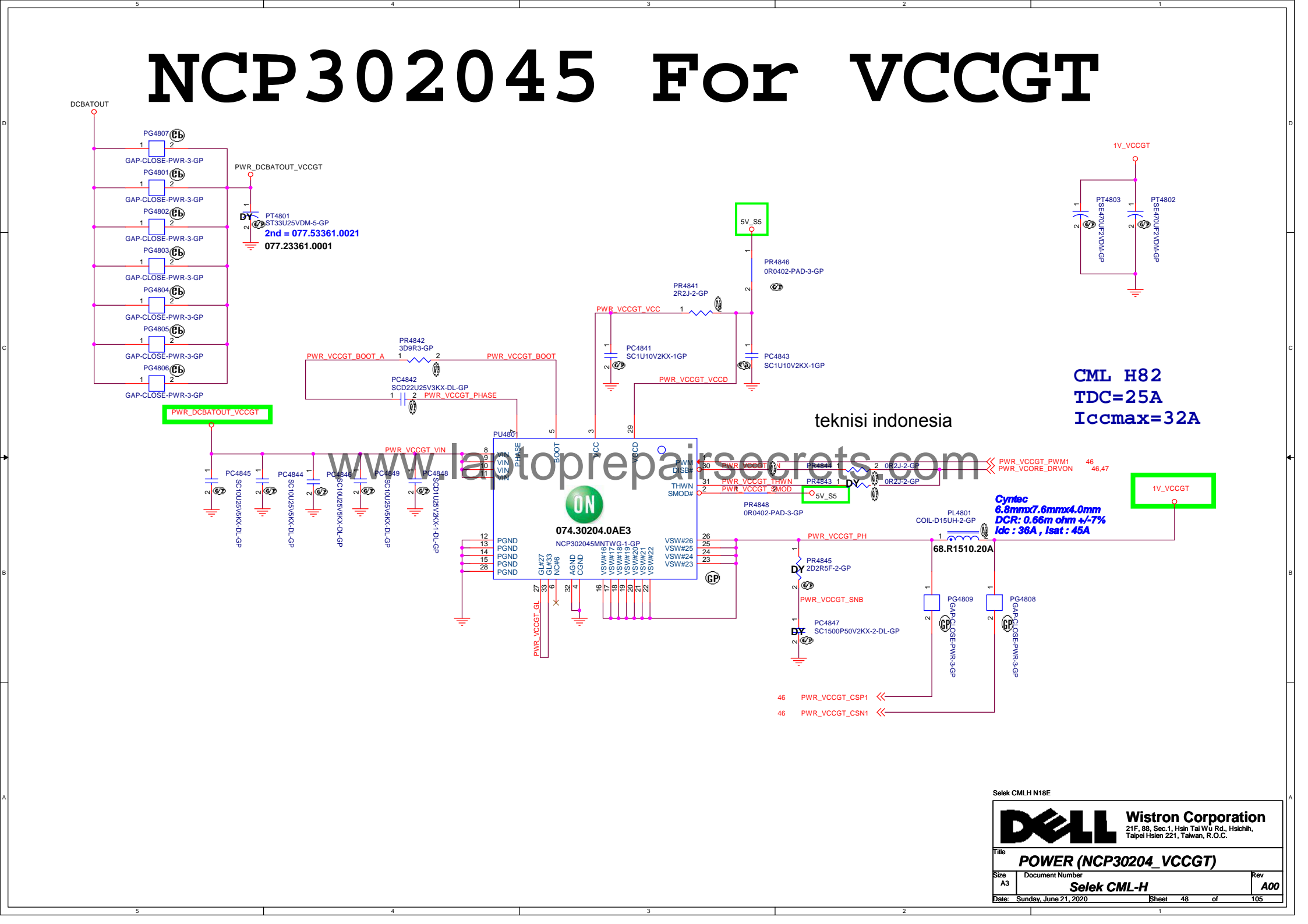


Phase5




Baseline	perf
PC4721	DV stuff
PC4724	DV stuff
PC4727	DV stuff
PC4728	DV stuff
PC4729	DV stuff
PC4735	DV stuff
PC4740	DV stuff
PC4745	DV stuff
PC4749	DV stuff
PC4750	DV stuff
PC4751	DV stuff
PC4752	DV stuff
PC4753	DV stuff
PC4754	DV stuff
PC4755	DV stuff

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[illegible][illegible]

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Title

Size
Custom

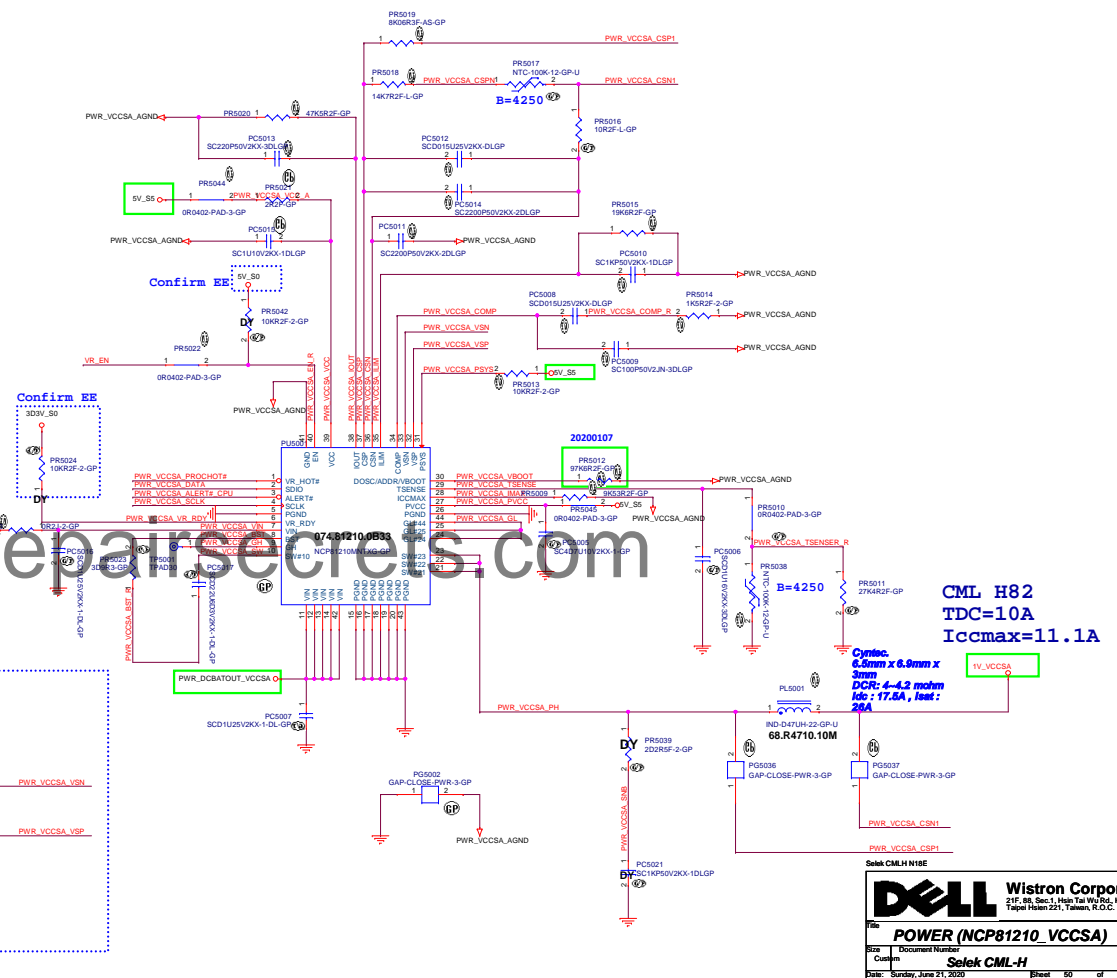
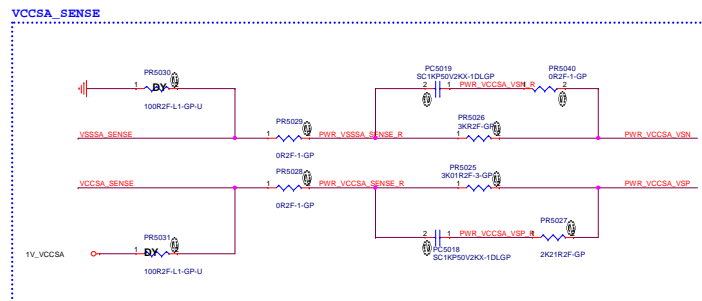
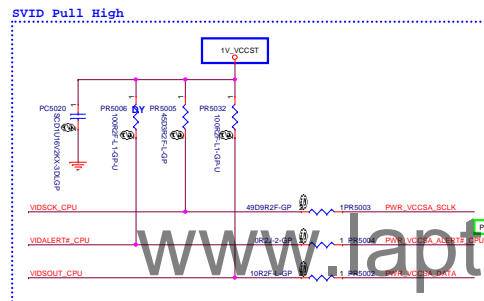
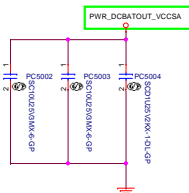
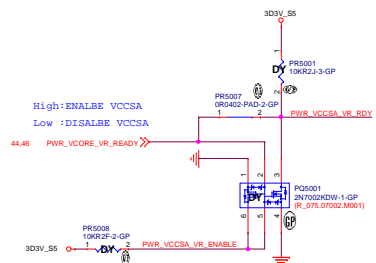
Document Number
Selek CML-H

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A00

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NCP81210 For VCCSA



CML H82
TDC=10A
Iccmax=11.1A

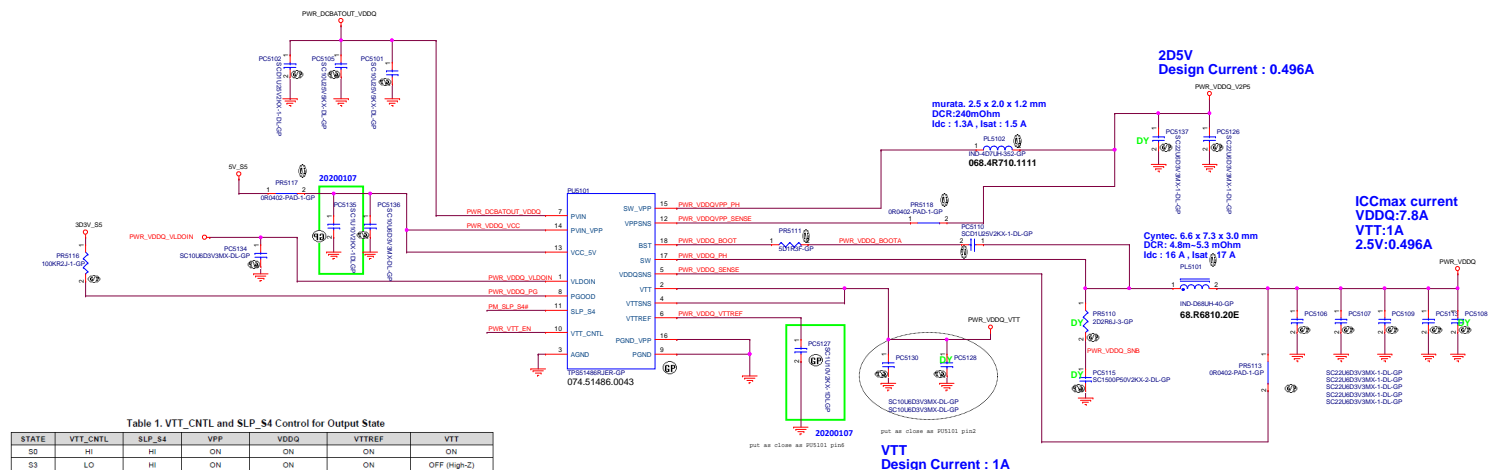
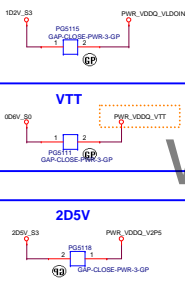
Cyntec.
6.5mm x 6.9mm x
3mm
DCR: 4~4.2 mohm
Idc : 17.5A , Isat :
26A

Selek CMLH N18E

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
POWER (NCP81210_VCCSA)			
Size	Document Number	Rev	
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The diagram illustrates the timing relationship between the S5 and S3 signals and the PHY on the EE side. The S5 signal (PM_SLM_S4M) is a square wave. The S3 signal (DDR_PG_OUT) is a square wave. The diagram shows the relationship between these signals and the PHY on the EE side, including PWR_VDDQ_RQ and PWR_VTT_EN signals.

Figure 1: Schematic representation of the two-dimensional network of the PWR. The diagram shows a grid of nodes (circles) connected by lines. The nodes are labeled with their IDs and the number of connections (degree) to adjacent nodes. The nodes are arranged in a grid with columns labeled 'DCBAT01' and 'PWR_DCBOAT01_VCC00' on the left, and 'ID2Y_B3' and 'PWR_VCC00' on the right. The nodes are connected in a grid pattern, with some nodes having additional connections to the right. The nodes are labeled with their IDs and the number of connections (degree) to adjacent nodes.

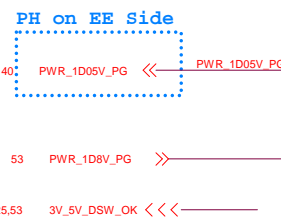


STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

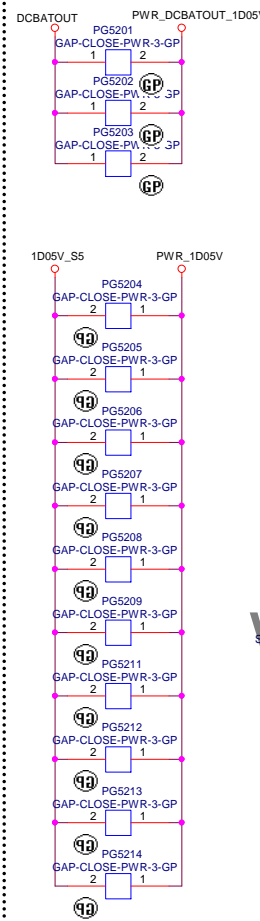
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SSID = PWR.Plane.Regulator_1D05V

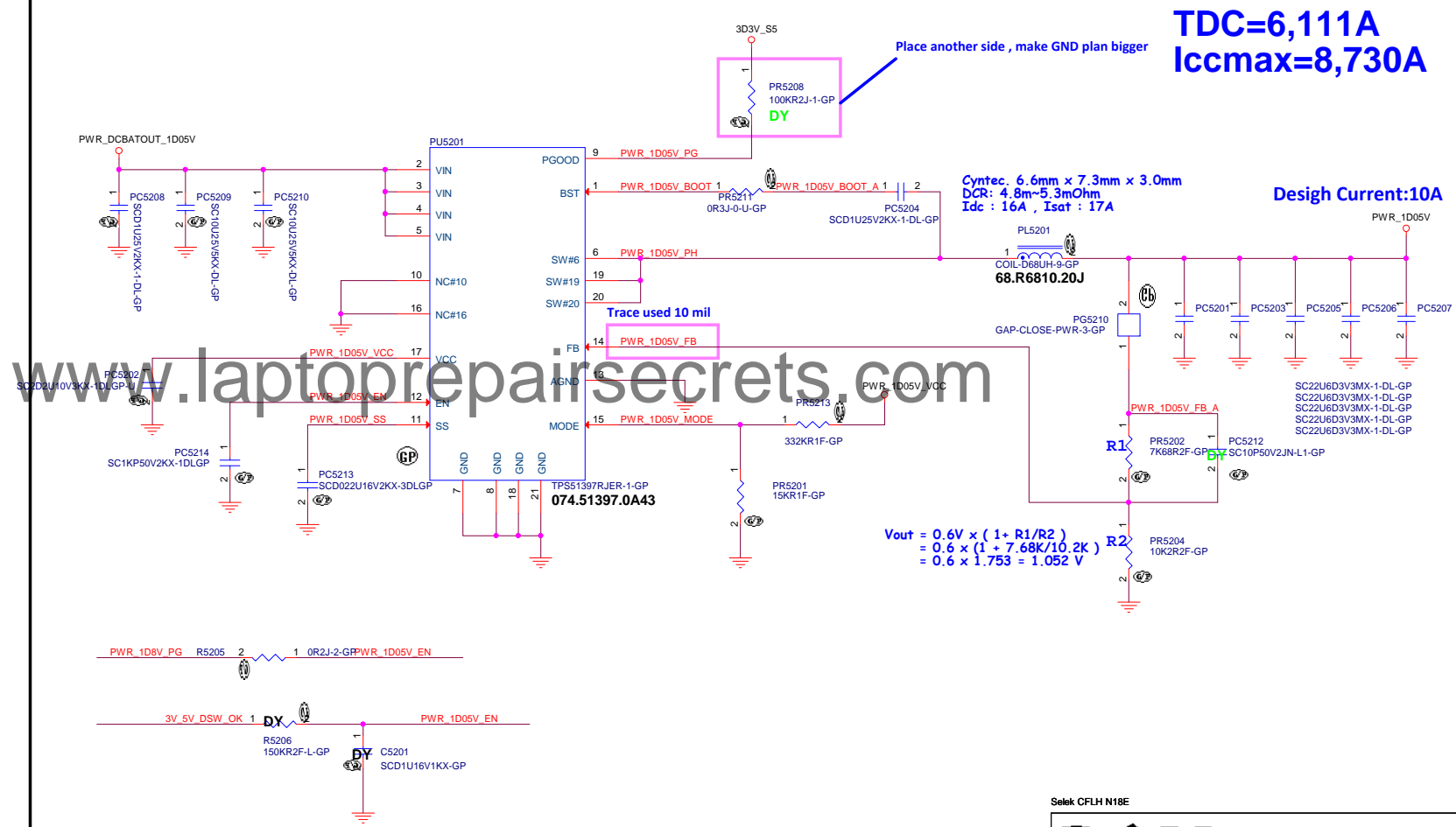
OFFPAGE-Signal



OFFPAGE-GAP



TPS51397 For 1D05V



Selek CFLH N18E

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Title **TPS51397_1D05V**

Size Custom Document Number **Selek CML-H** Rev **A00**

Date: Sunday, June 21, 2020 Sheet 52 of 105

Main Func = 1D8V

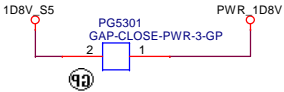
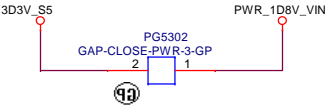
OFFPAGE

25,52 3V_5V_DSW_OK >>

PH on EE Side

52 PWR_1D8V_PG << PWR_1D8V_PG

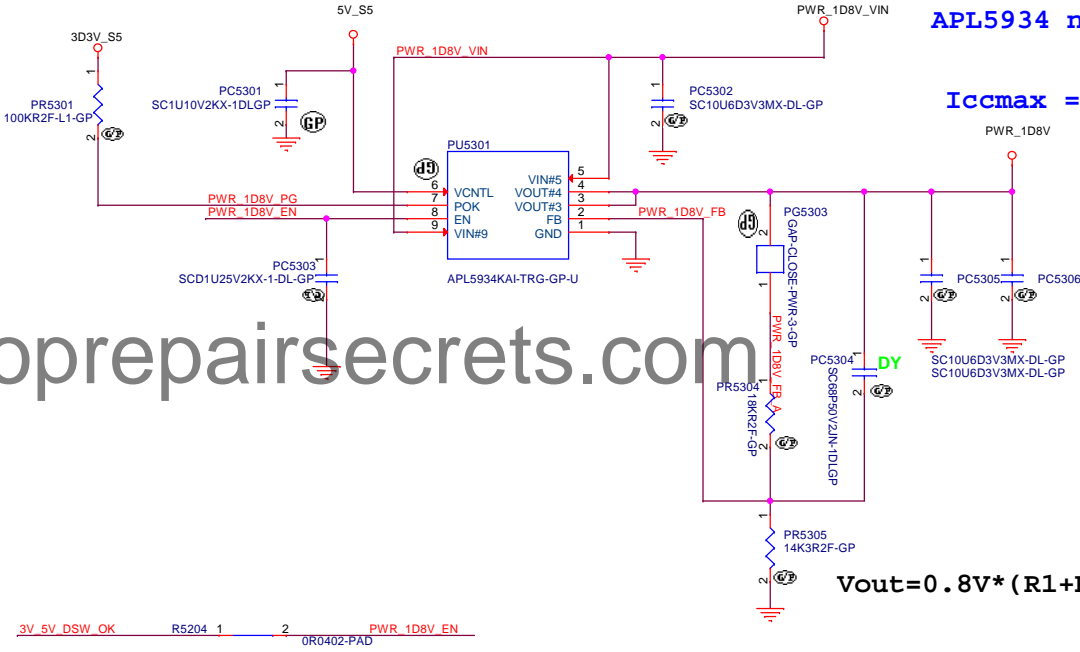
OFFPAGE_GAP



APL5934 for 1D8V

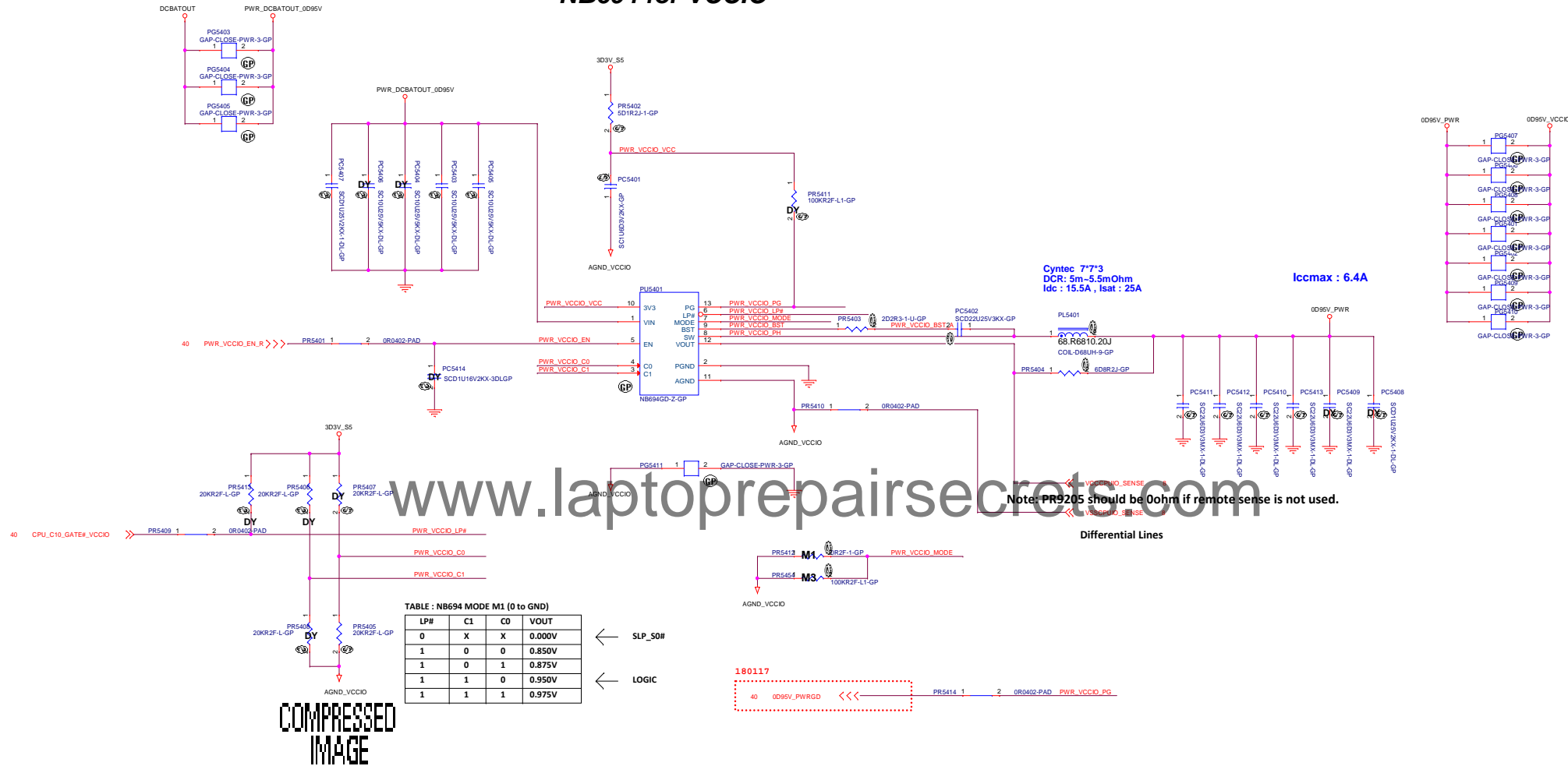
APL5934 need <1.8W

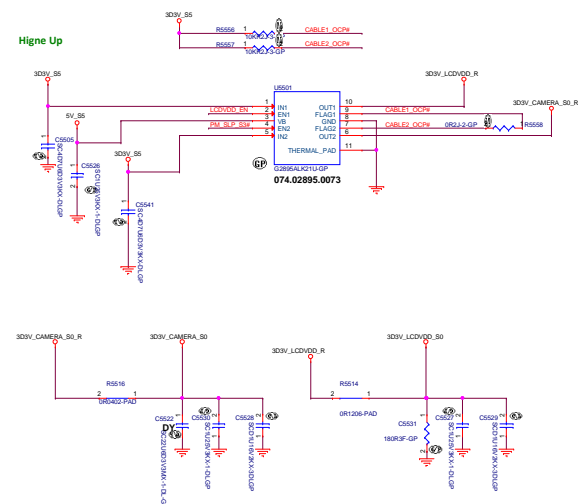
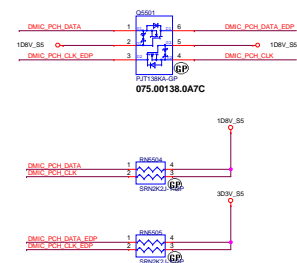
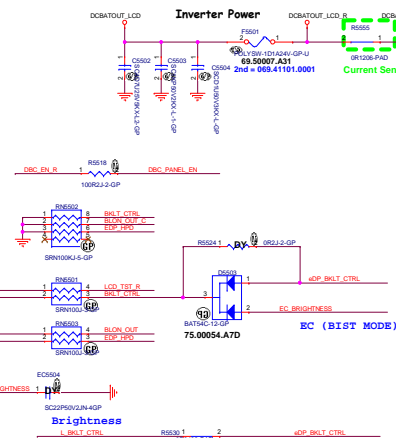
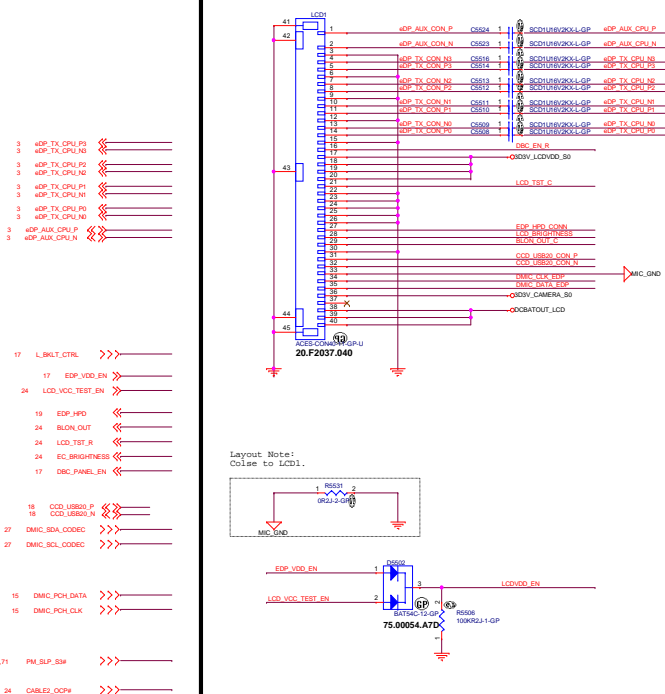
Iccmax = 152mA



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NB694 for VCCIO



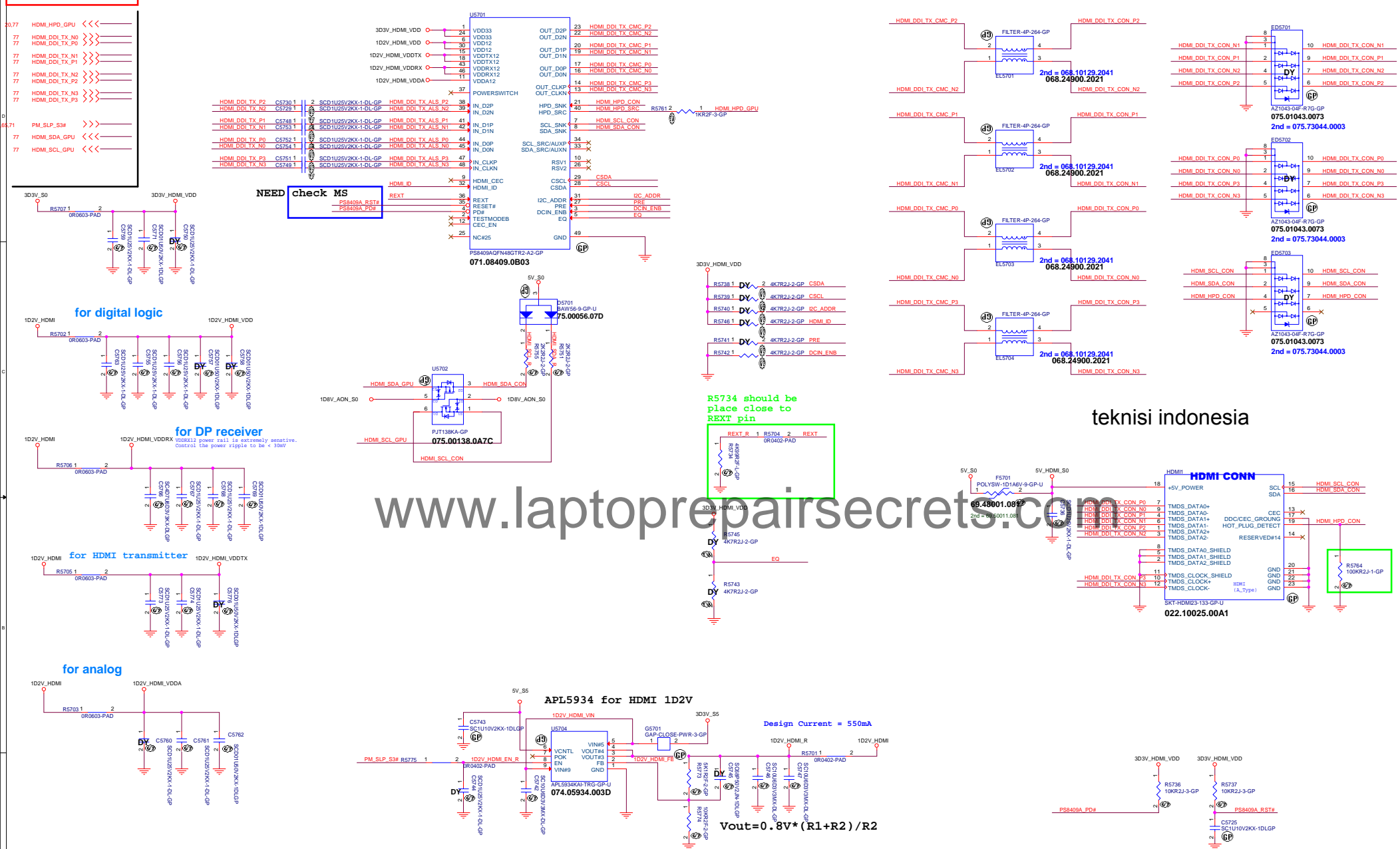


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Selek CMLHN16E

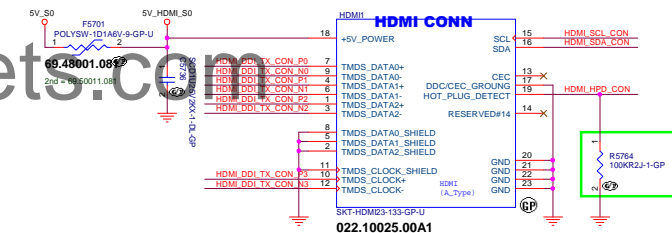
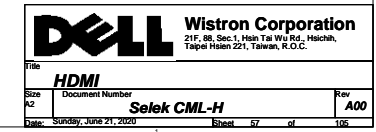
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD/Inverter Connector			
Size Custom	Document Number Selek CML-H		Rev A00
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SSID = HDMI

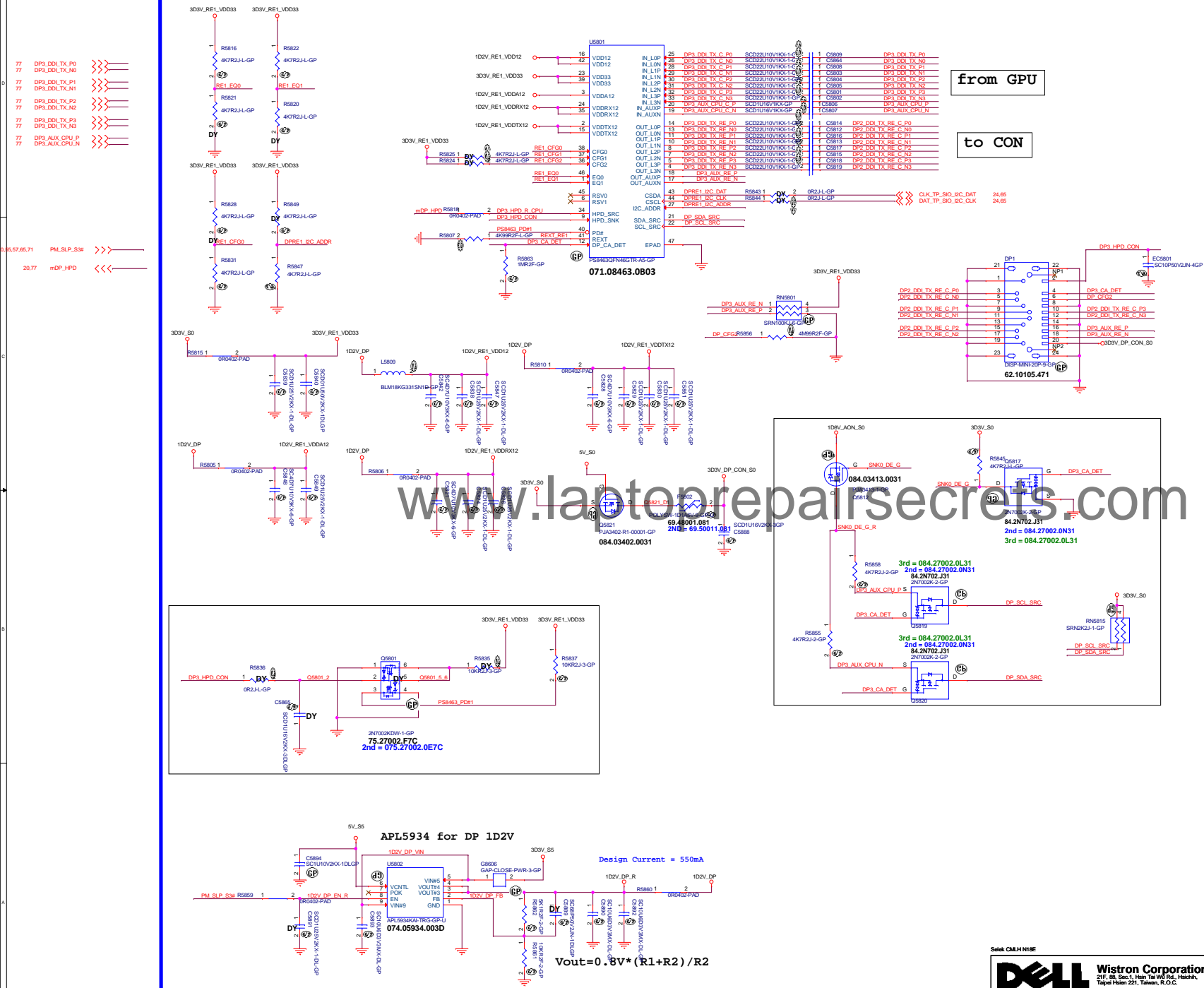


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DP
Re-driver




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Title (Reserved)			
Size A	Document Number Selek CML-H		Rev A00
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Title

SATA HDD

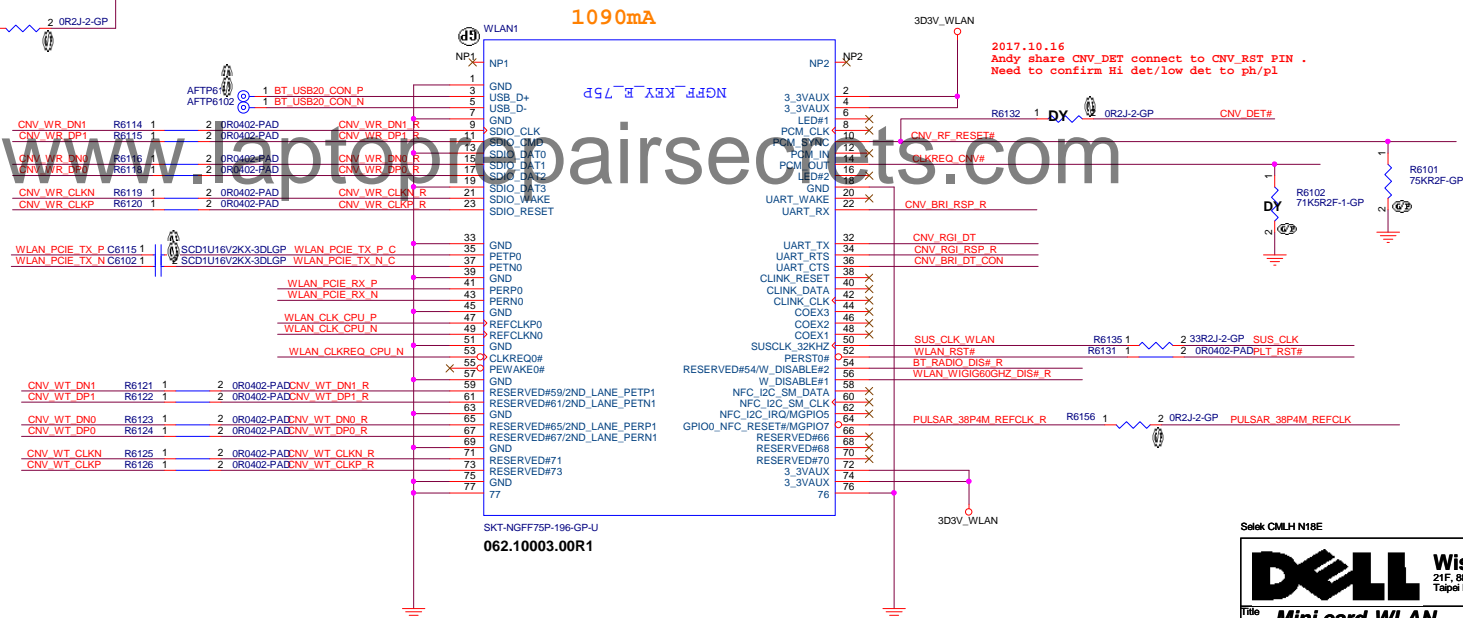
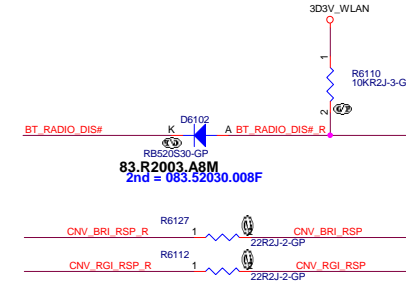
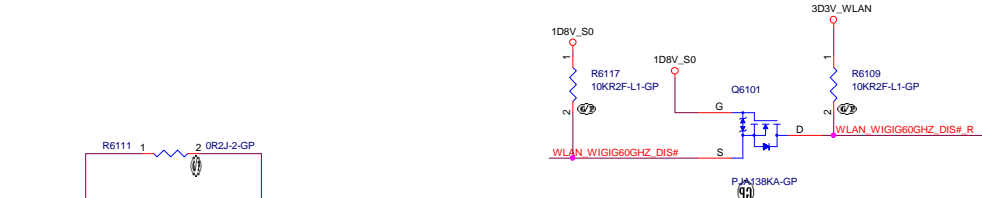
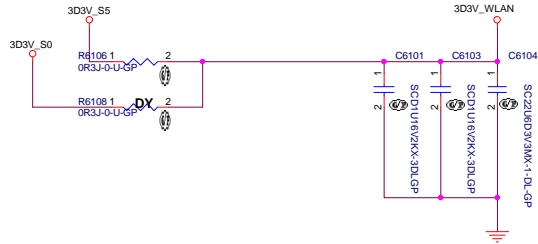
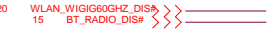
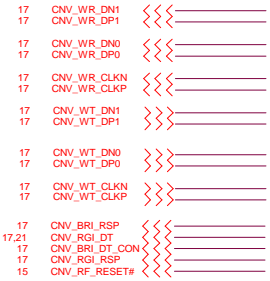
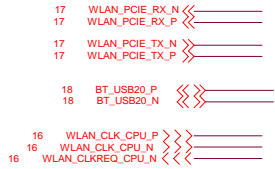
Size
Custom

Document Number
Selek CML-H

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A00

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Main Func = WLAN




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Select CMLH N18E			
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Mini card-WLAN			
Size	Document Number	Rev	
Custom	Select CML-H	A00	
Date:	Sunday, June 21, 2020	Sheet 61 of	105

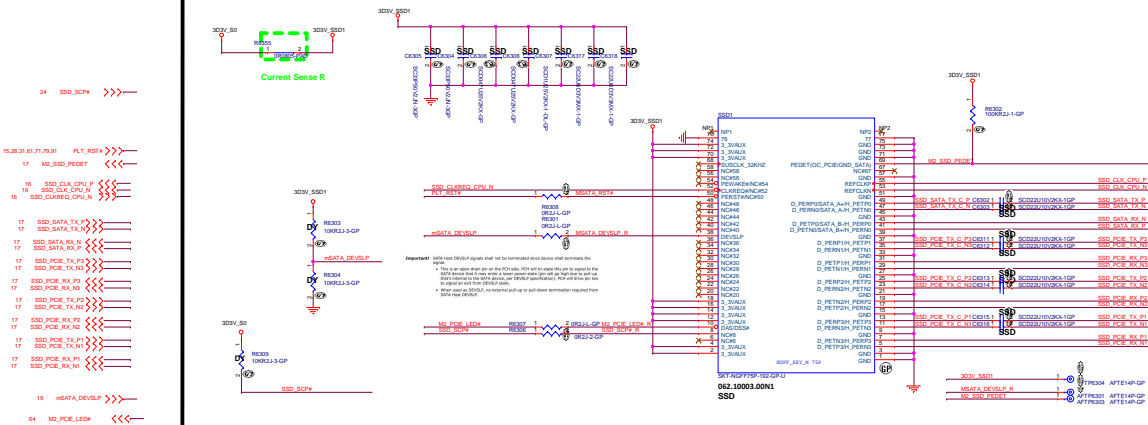
SSID = Wireless

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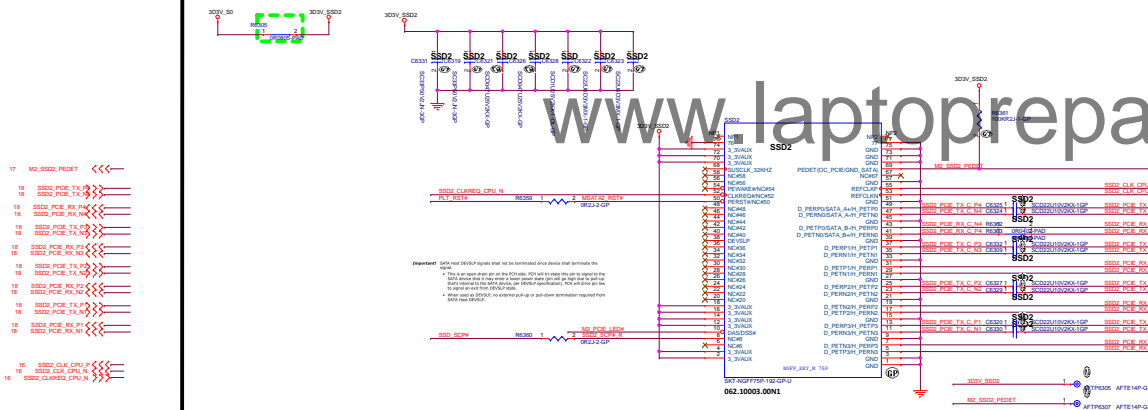
Selek CMLH N18E

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Title (Reserved)WWAN			
Size A	Document Number Selek CML-H		Rev A00
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Mini Card Connector (NGFF m-SATA) SSD



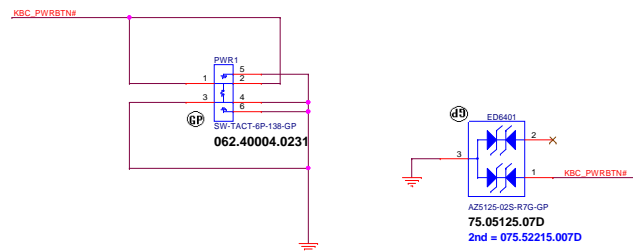
Mini Card Connector (NGFF m-SATA) SSD2



SSID = User.Interface

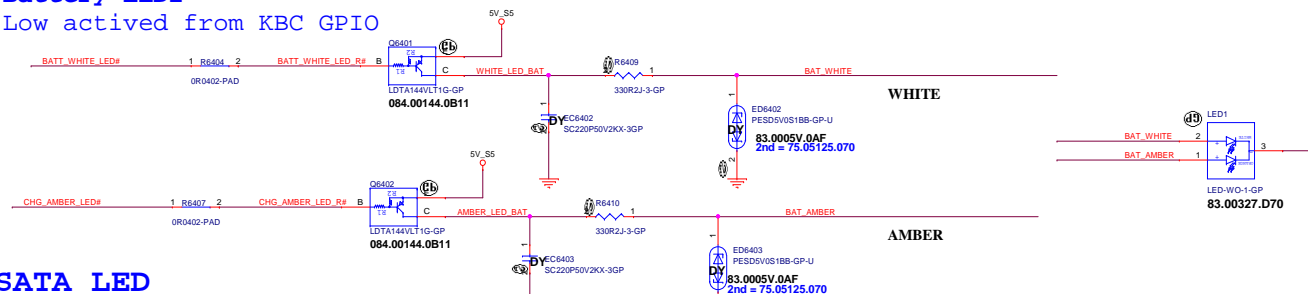
Power button

NONE FINGER PRINT 0-0 | HWY6

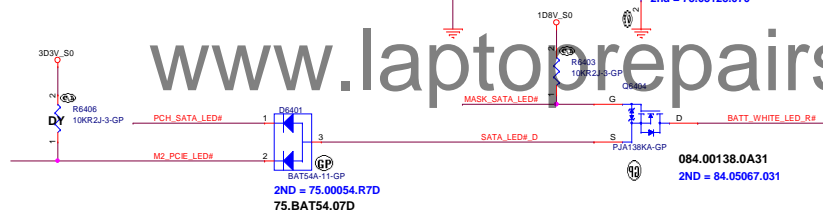


Battery LED1

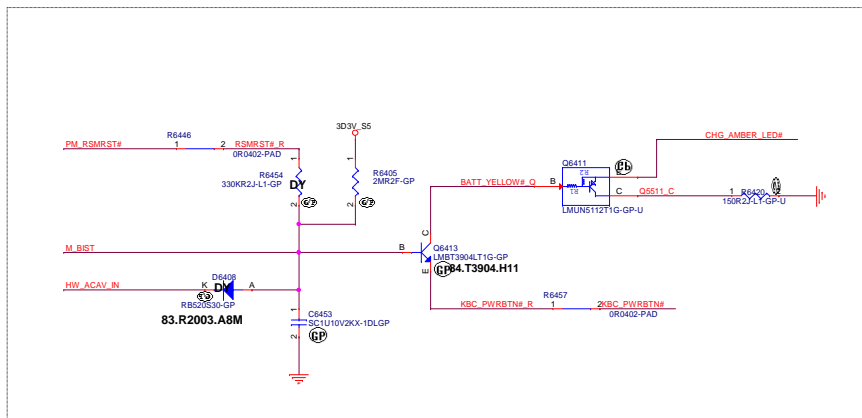
Low activated from KBC GPIO



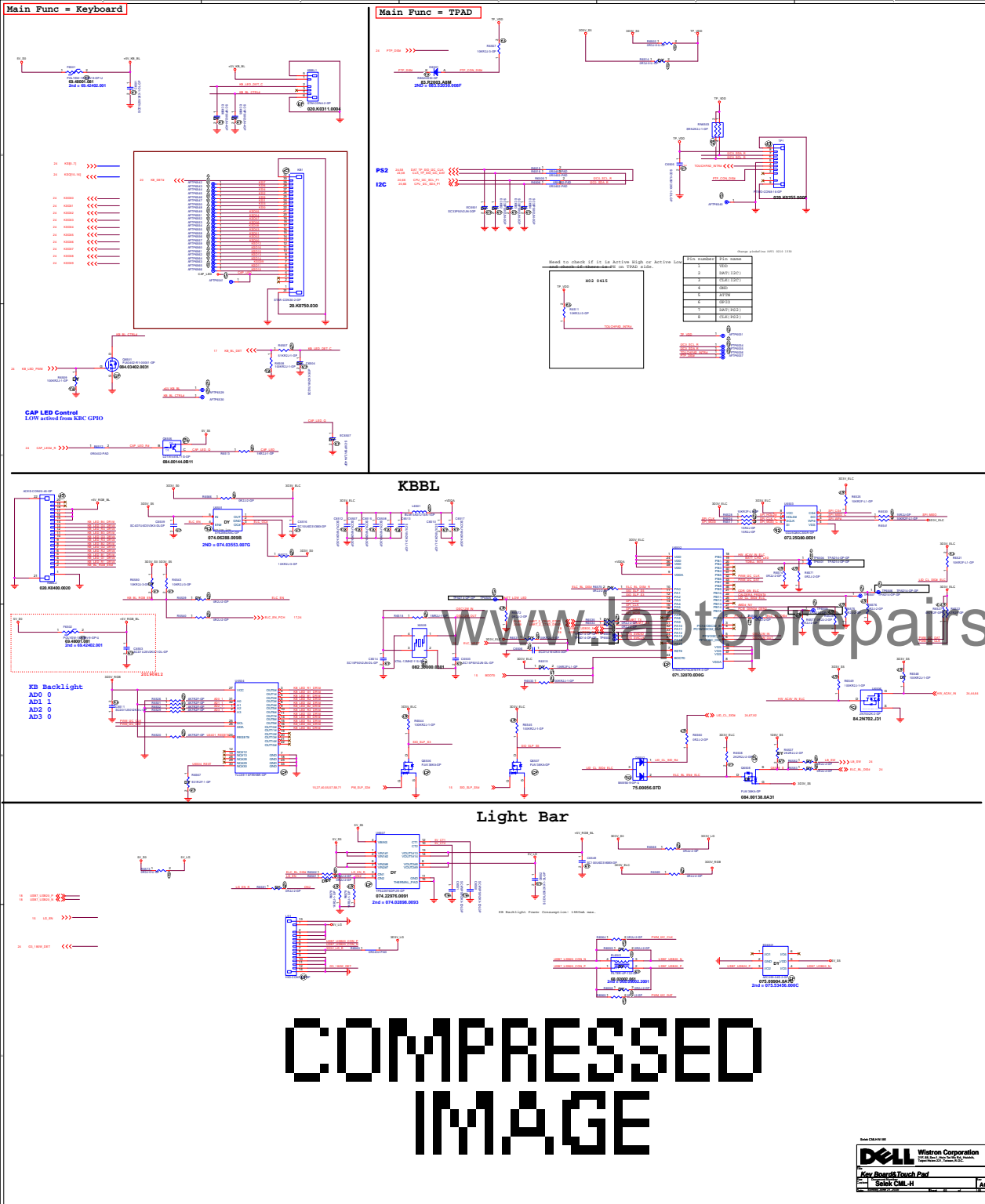
SATA LED



M-BIST for G10 (Proposed schematic)
follow bandon



Selek CML/H N18E

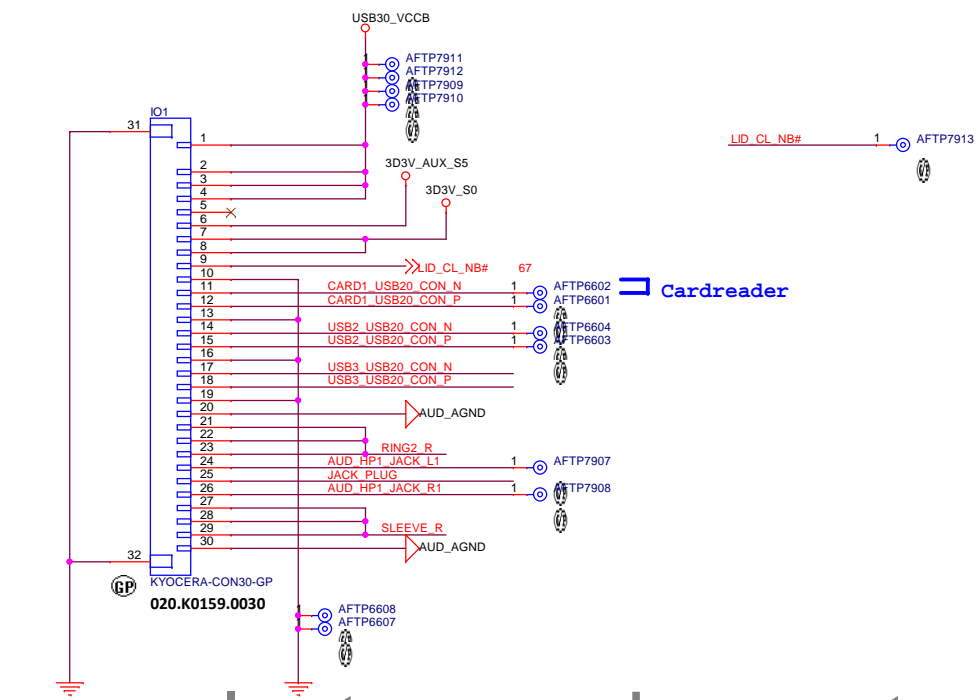


18 USB3_USB20_P >>>
 18 USB3_USB20_N >>>
 18 USB2_USB20_P >>>
 18 USB2_USB20_N >>>
 18 CARD1_USB20_P >>>
 18 CARD1_USB20_N >>>

29 RING2_R >>>
 29 AUD_HP1_JACK_L1 >>>
 29 JACK_PLUG >>>
 29 AUD_HP1_JACK_R1 >>>
 29 SLEEVE_R >>>

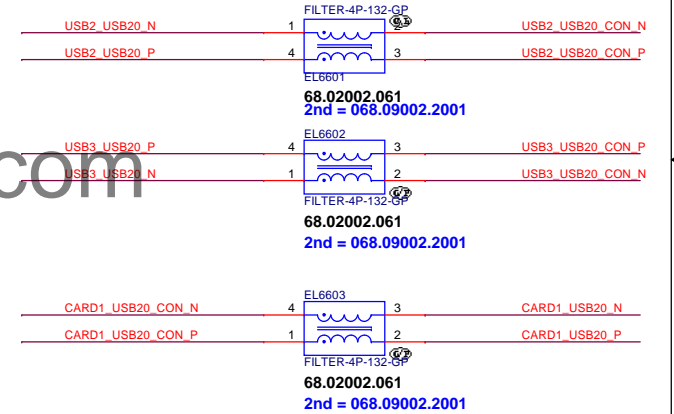
20.65 CPU_I2C_SCL_P1 >>>
 20.65 CPU_I2C_SDA_P1 >>>

44 BT_PWR_IN+ >>>
 44 BT_PWR_IN- >>>

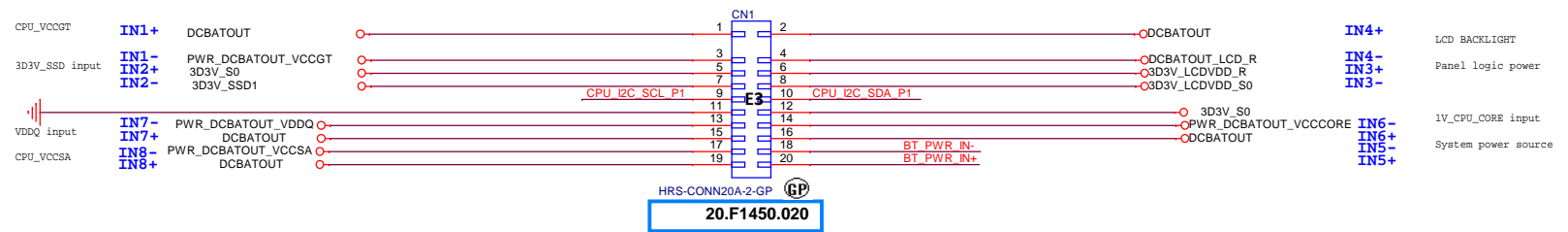


Cardreader

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E3 reserve



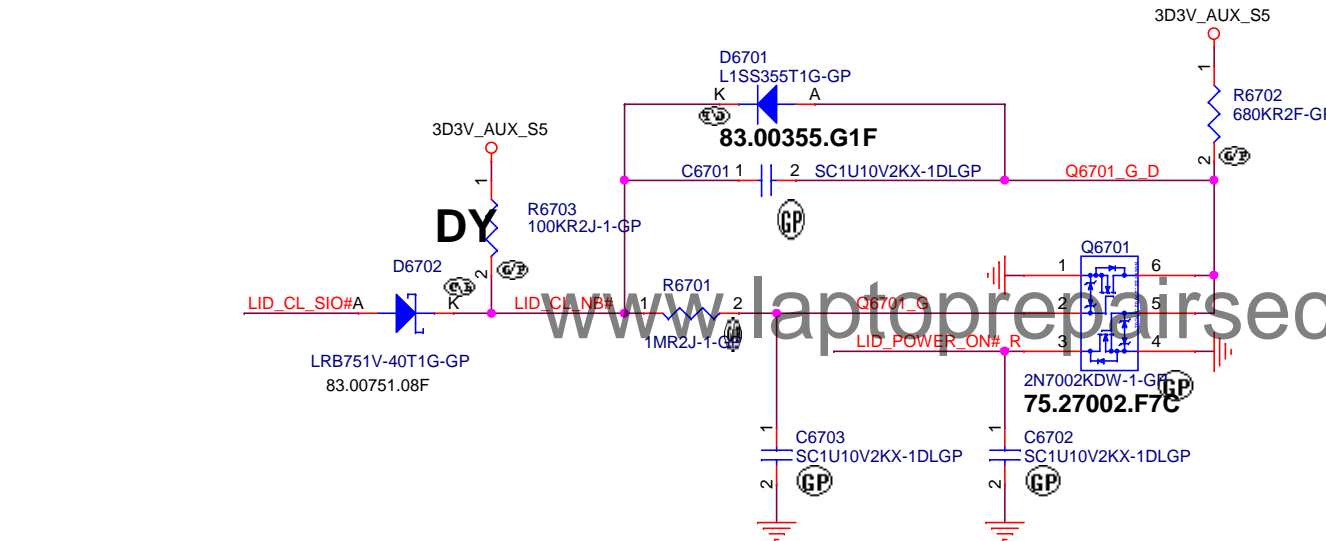
Selek CMLH N18E



Title IO Board Connector		
Size A3	Document Number Selek CML-H	Rev A00
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Main Func = Hall Sensor

24	LID_POWER_ON#_R	>>>_____
24,65,92	LID_CL_SIO#	<<<_____
66	LID_CL_NB#	<<<_____



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Taipei Hsien 221, Taiwan, R.O.C.

Title	Hall Sensor
-------	--------------------

Size	Custom
------	--------

Document Number
Selek CML-H

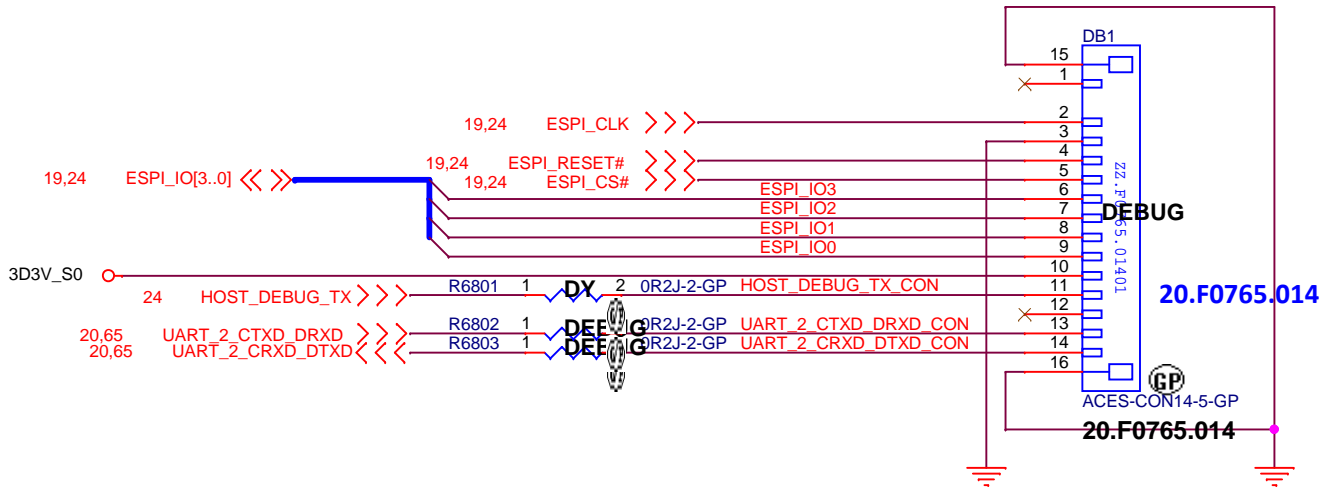
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Main Func = Debug

Debug Connector




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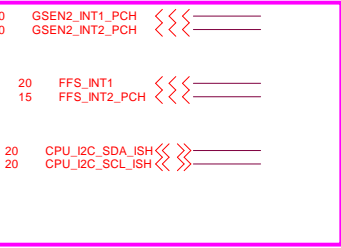
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number Selek CML-H		Rev A00
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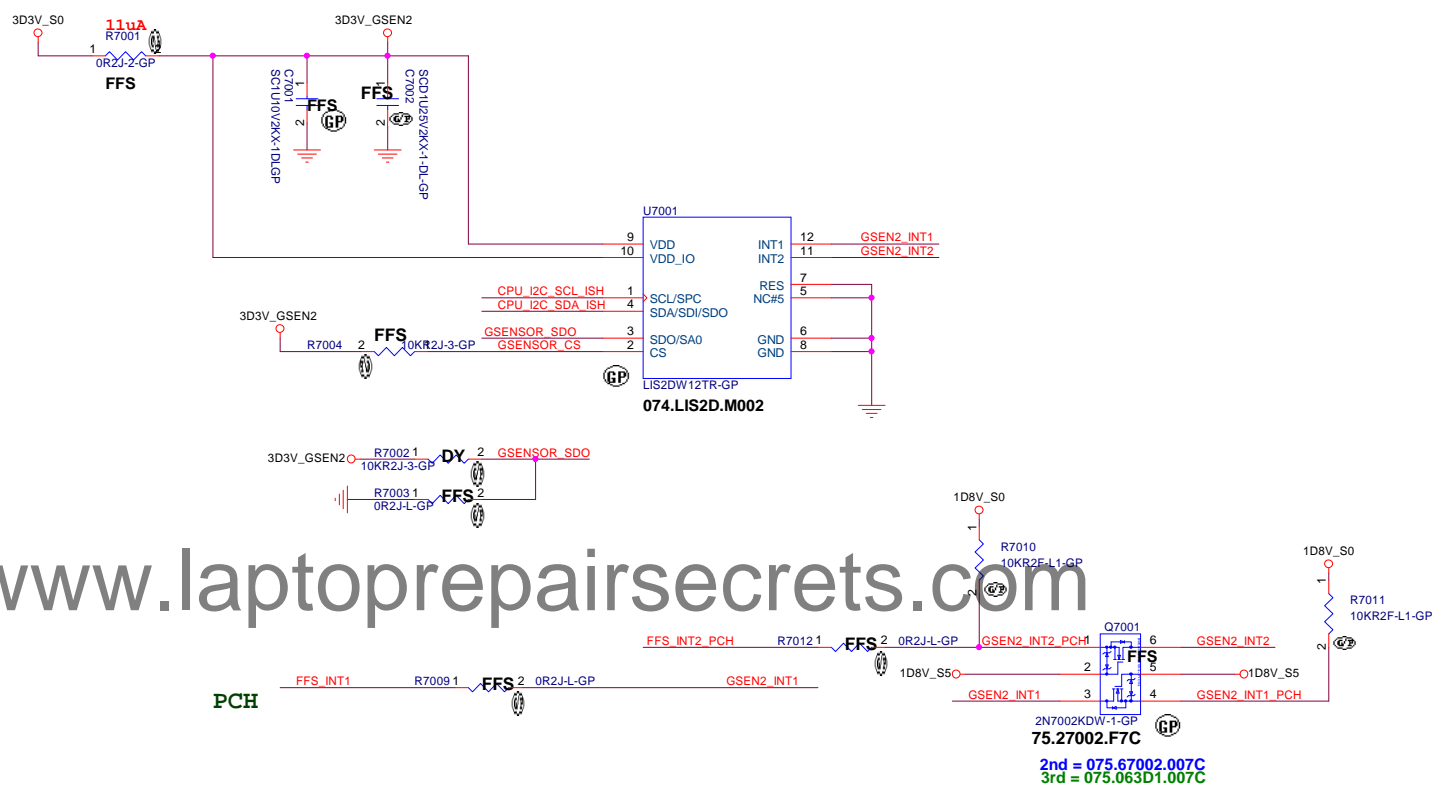
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number Selek CML-H		Rev A00
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SSID = Free Fall Sensor



20180726 need DELL GPIO table

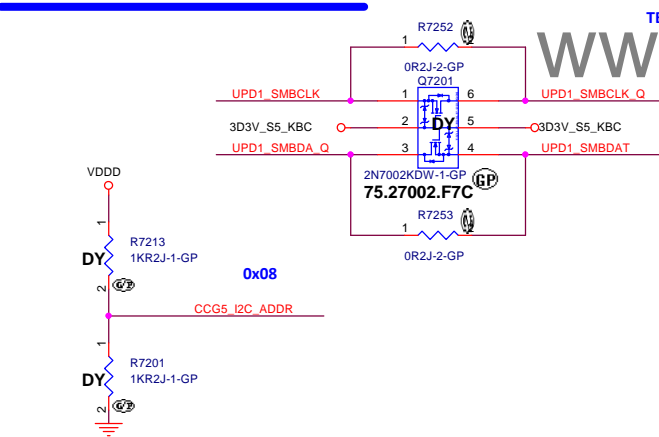
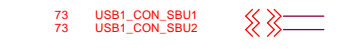
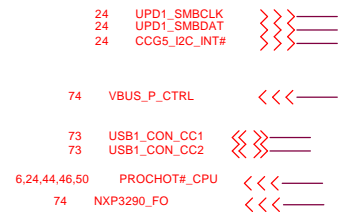
Free Fall Sensor + G Sensor



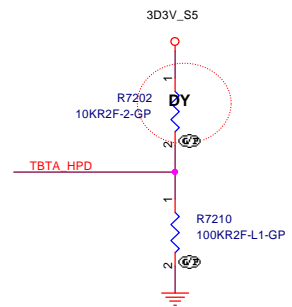
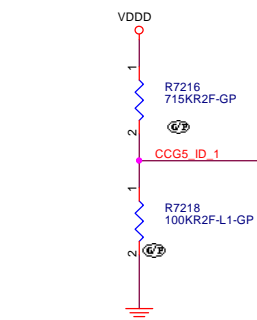
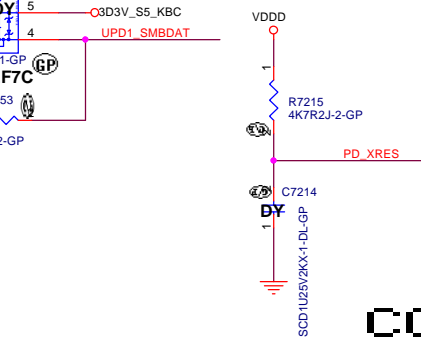
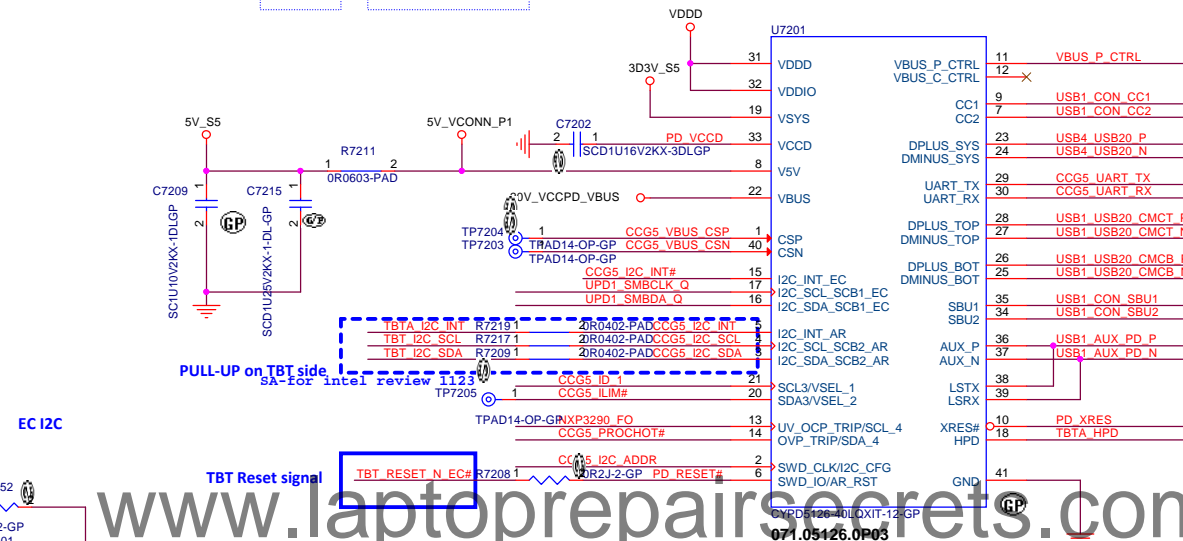
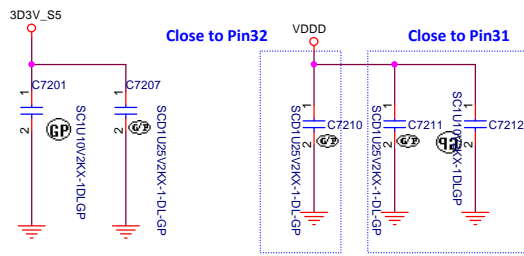
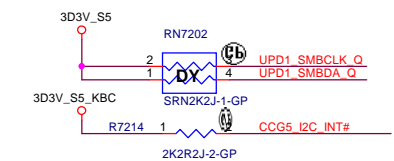
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Main Func = TypeC



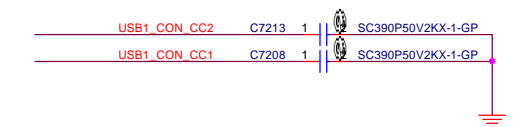
CCG5's I2C address is decided by the SWD clock pin.
Don't mount R8 and R9 for the I2C address 0x08. This is the default one.
Mount only R9 for the I2C address 0x40.
Mount only R8 for the I2C address 0x42.



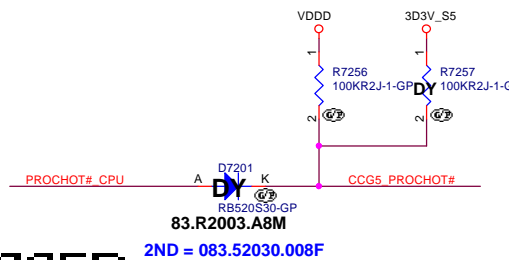
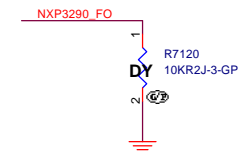
```

PD Function
Normal: High
Active : Low

```



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COMPRESSED
IMAGE

COMPRESSED IMAGE

For Debug

**Selek CMLH N18E**

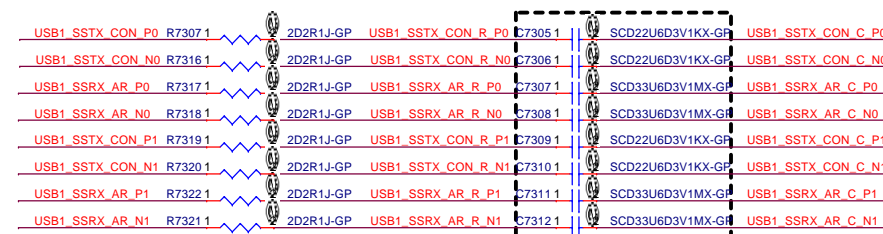
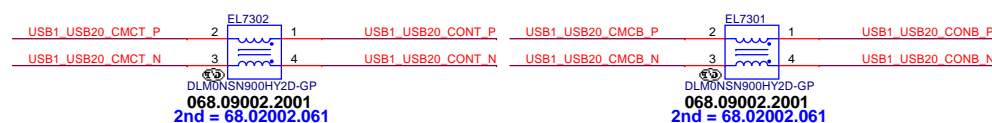
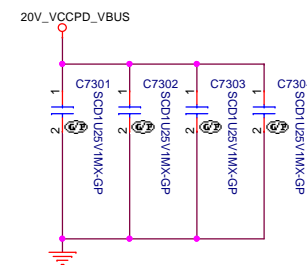
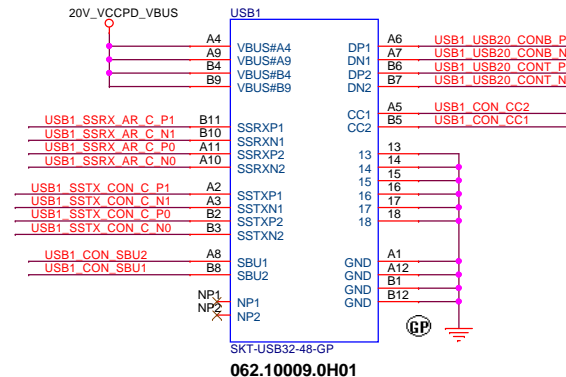
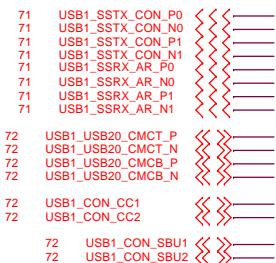
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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EXT IO (Thunderbolt(2/3)/Type C CC Logic)

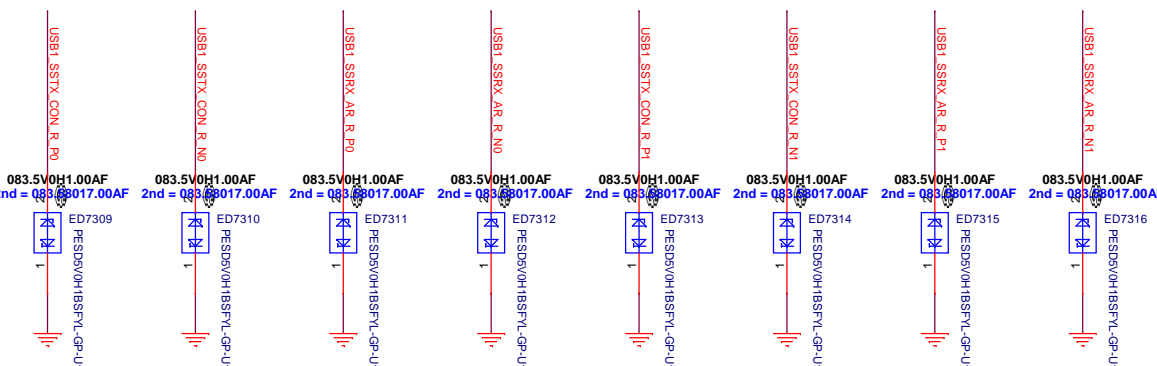
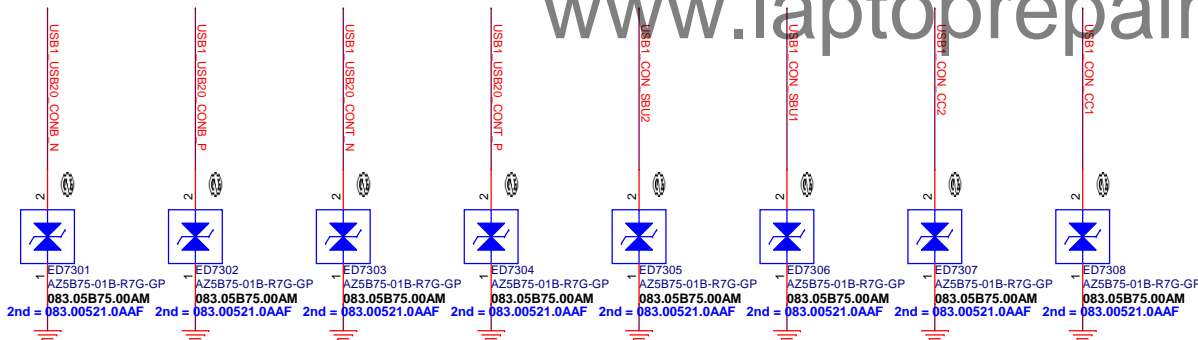
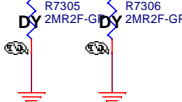
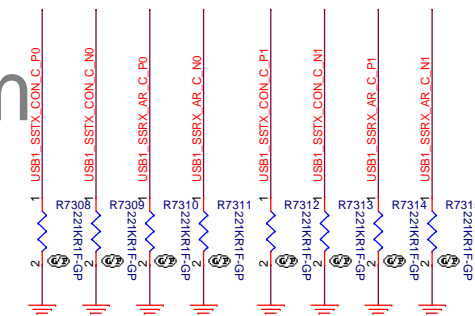
Size A3	Document Number Selek CML-H	Rev A00
Date: Sunday, June 21, 2020	Sheet 72 of	105

```
Main Func = TypeC
```

USB1



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Wistron Corporation
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Title **EXT IO (Thunderbolt(3/3)/Type C Conn)**

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Main FUNC = LPS

72 VBUS_P_CTRL >>>

72 NXP3290_FO >>>

Form PD control


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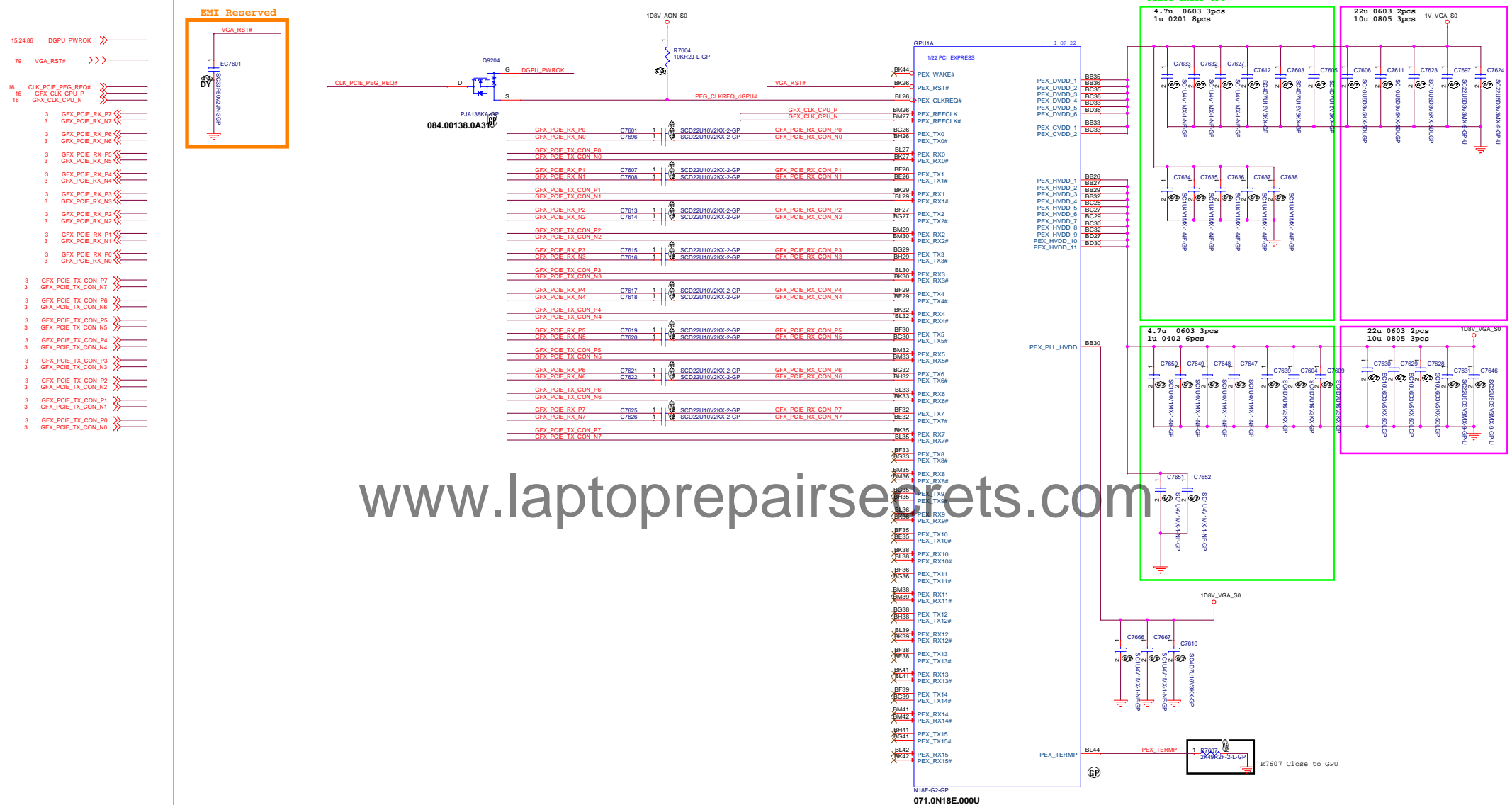
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File GPU(2/5)DIGITALOUT		
Size	Document Number	Rev
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Title (Reserved)Thunderbolt (5/5)			
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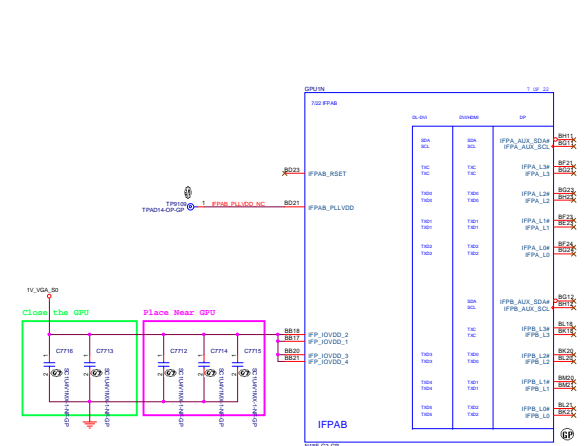
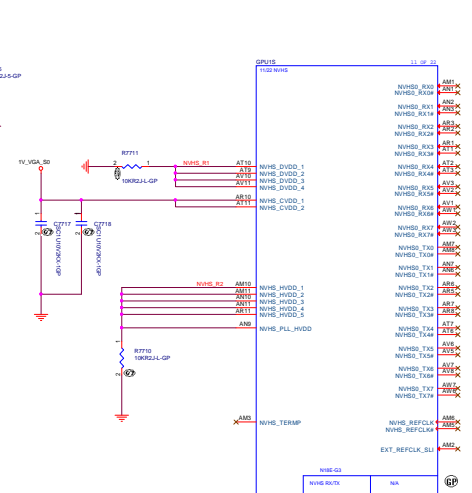
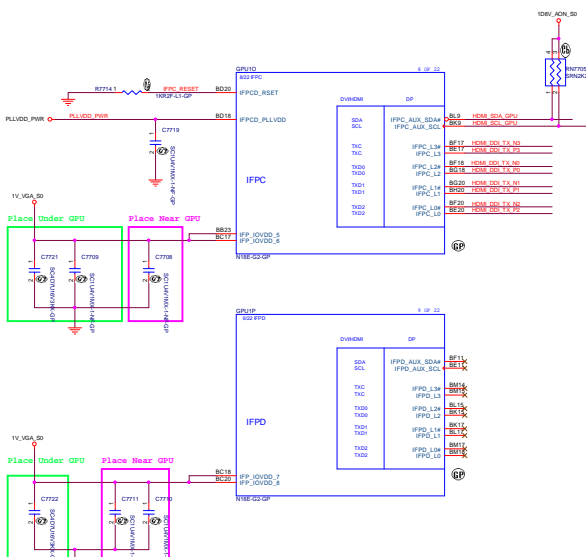


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Main Func = dGPU

25:57 HDMI_HPD_GPU >>>
57 HDMI_D0_TX_N0 <<<
57 HDMI_D0_TX_P0 <<<
57 HDMI_D0_TX_N1 <<<
57 HDMI_D0_TX_P1 <<<
57 HDMI_D0_TX_N2 <<<
57 HDMI_D0_TX_P2 <<<
57 HDMI_D0_TX_N3 <<<
57 HDMI_D0_TX_P3 <<<
57 HDMI_SCL_GPU <<<
57 HDMI_SCL_GPU <<<
75 GPIO27_IPFC_HPD <<<

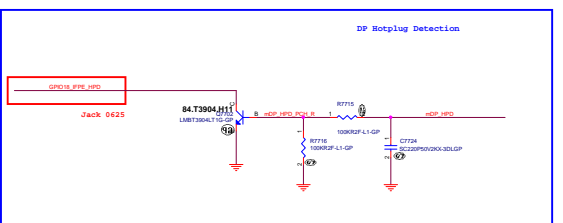
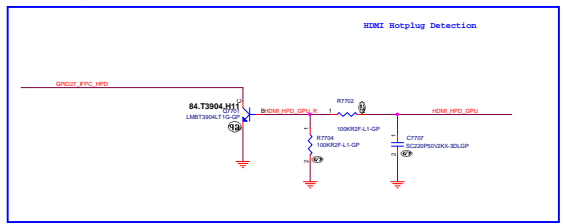
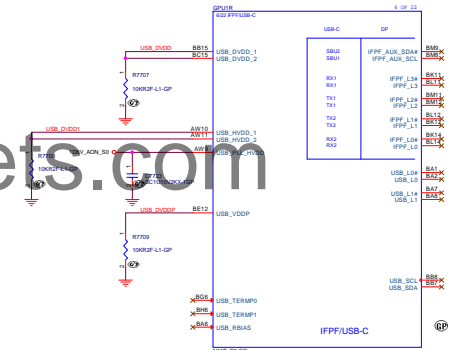
58 DPL_AUX_GPU_N <<<
58 DPL_AUX_GPU_P <<<
58 DPL_D0_TX_N0 <<<
58 DPL_D0_TX_P0 <<<
58 DPL_D0_TX_N1 <<<
58 DPL_D0_TX_P1 <<<
58 DPL_D0_TX_N2 <<<
58 DPL_D0_TX_P2 <<<
58 DPL_D0_TX_N3 <<<
58 DPL_D0_TX_P3 <<<
25:59 dGPU_HPD >>>
75 GPIO18_IPFE_HPD <<<



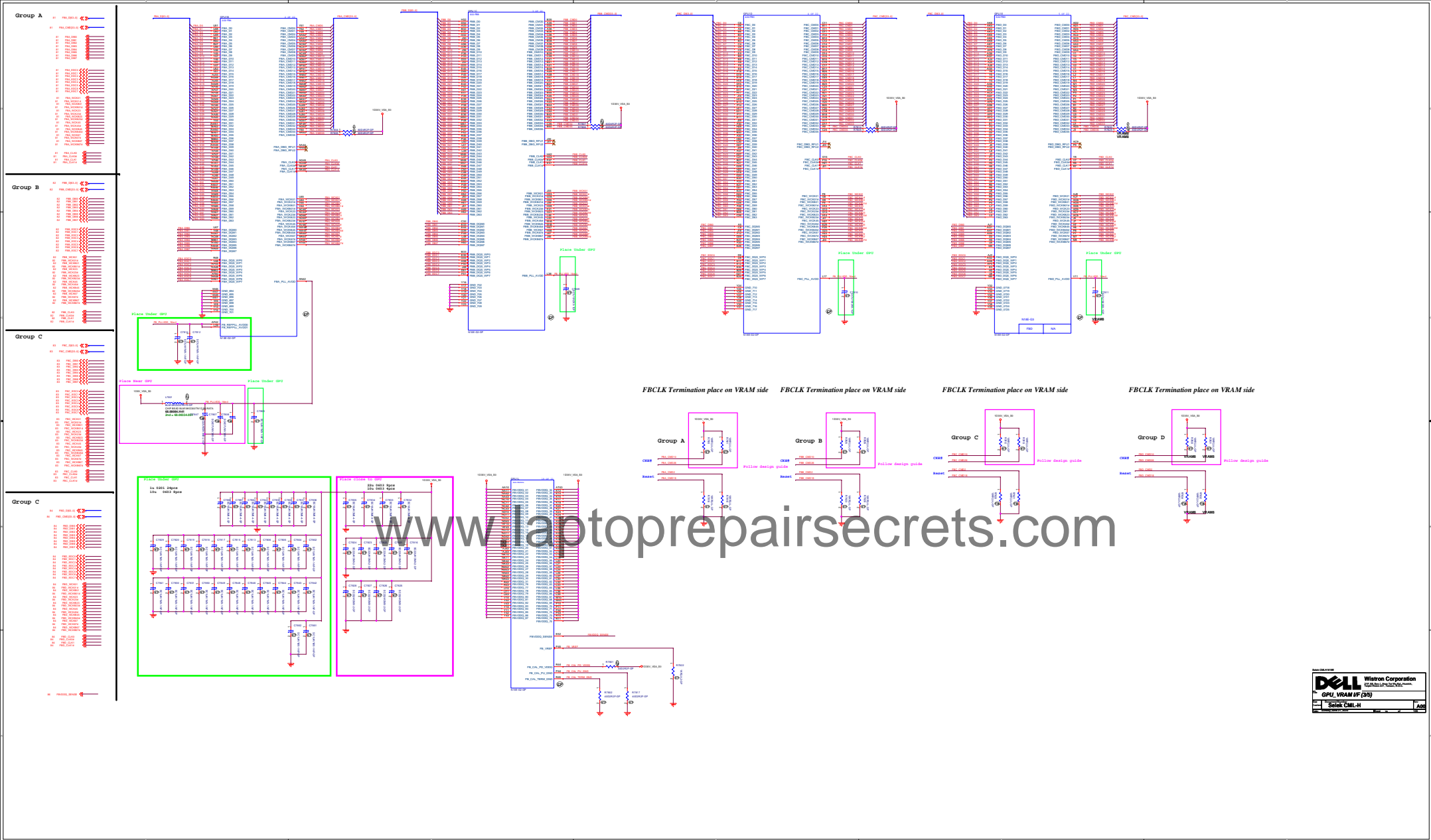
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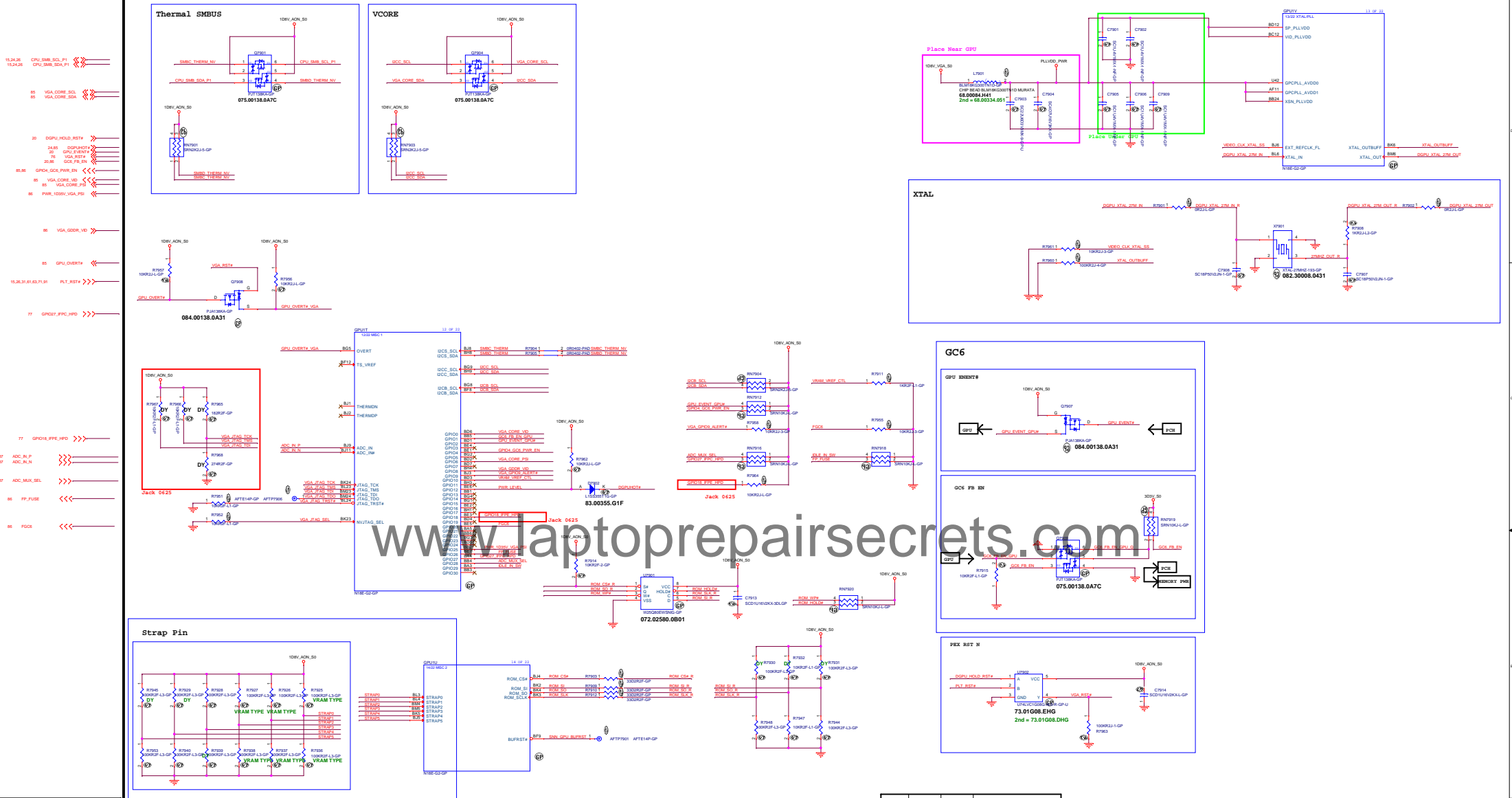
Table 9.1 Display Link Summary (GB4B-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort	USBC
If USB-C is implemented					
IFPA (Link A)	✓(Dual Link with IFPA)			✓	
IFPB (Link B)	✓(Dual Link with IFPA)			✓	
IFPC (Link C)		✓		✓	
IFPD (Link D)			✓		
IFPE (Link E)					✓
IFPF (Link F)					✓



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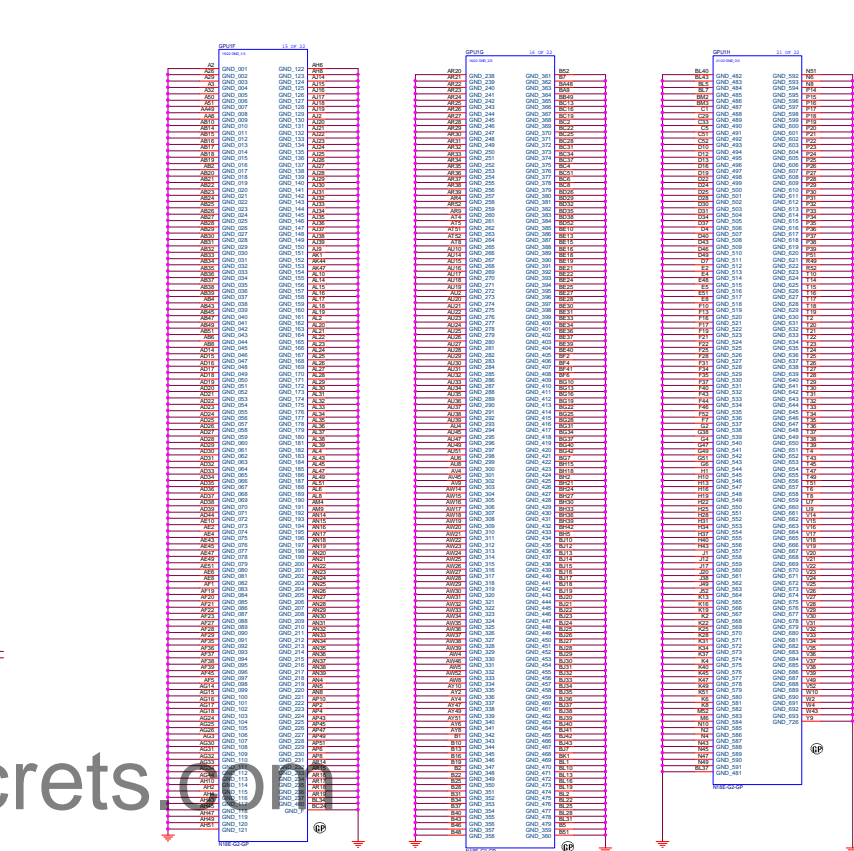
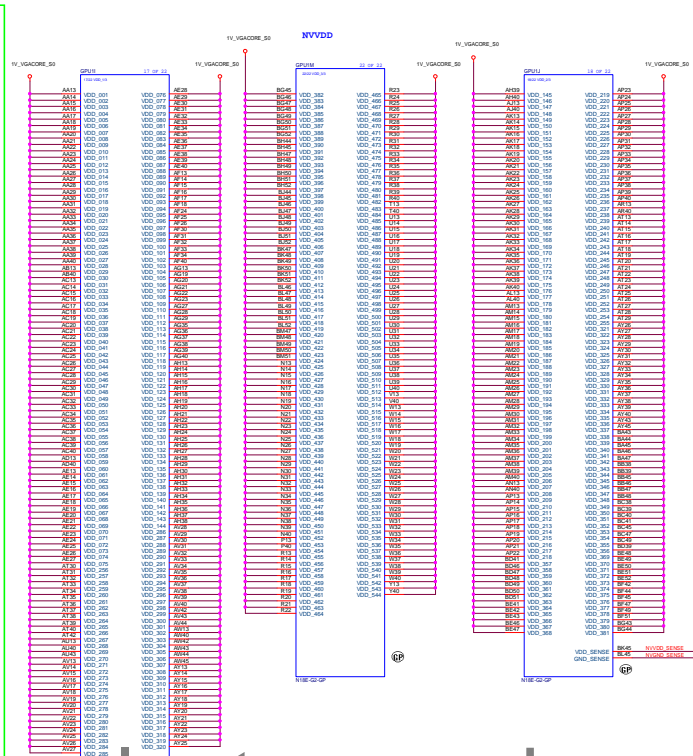
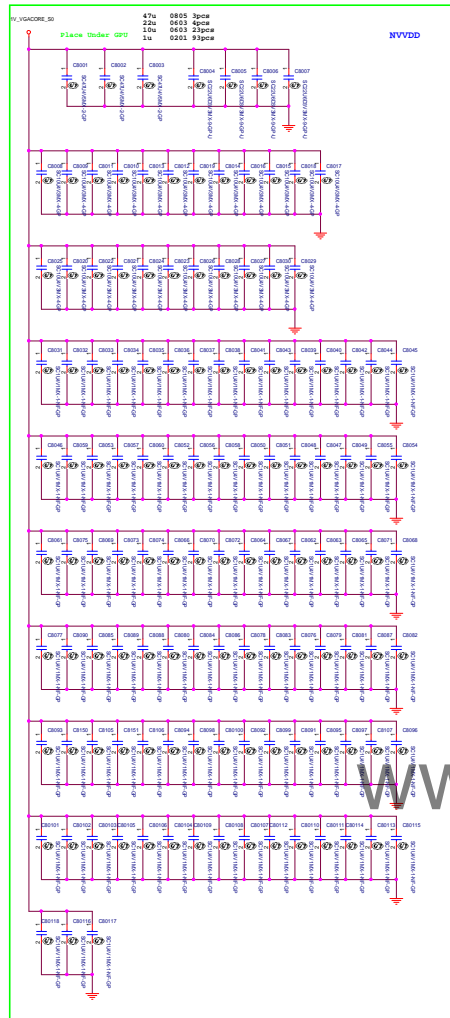
MEMORY STRAP

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

Table 2. N18E-G2/G1 GDDR6 Recommended Memories									
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V ¹	Micron	MT61K256M32JE-14-A	A-die	0x1	14 Gbps	N/A	Full Production candidate
Notes:									
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.									
2. DVS is required. WCLK: TBD									
Table 3. N18E-G0 GDDR6 Recommended Memories									
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V ¹	Samsung	K4Z803258C-HC14	C-die	0x0	14 Gbps	N/A	Full Production candidate
Notes:									
1. For N18E-G0, the maximum allowable memory case temperature is 95 °C.									
2. DVS is required. WCLK: TBD									

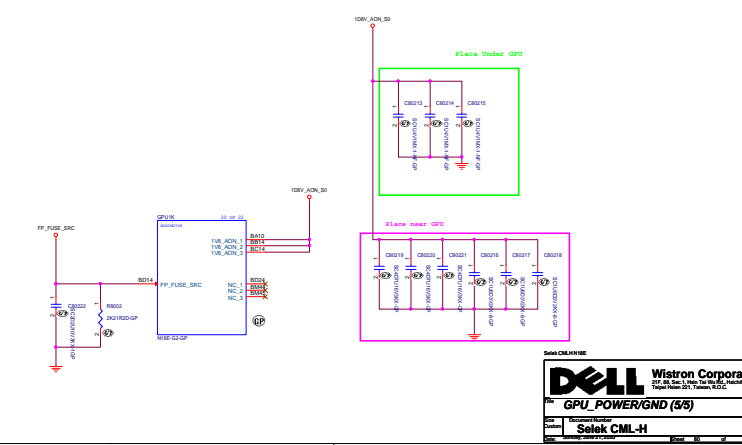
STRAP5	STRAP4	STRAP3	Function
L	L	H	as below picture

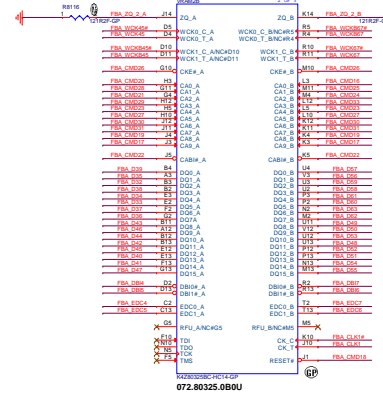
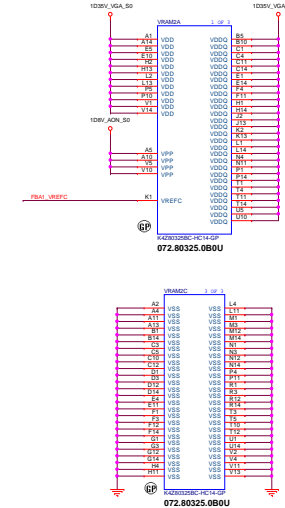
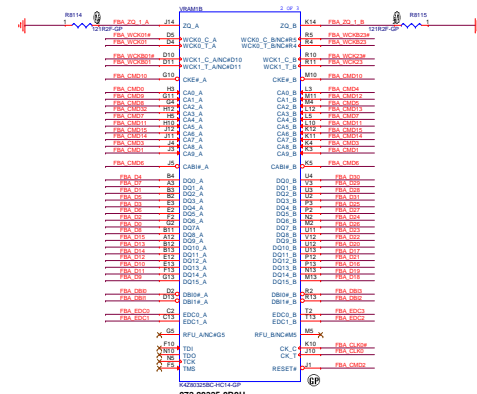
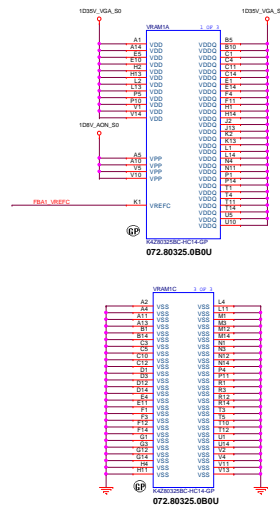
Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE					
Strap Pins See Note			Functions Selected by This Strapping		
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	0	1
L	H	H	0	0	1
H	L	L	0	1	0
H	L	H	0	1	0
H	H	L	0	1	1
H	H	H	0	1	1
L	L	M	1	0	0
L	M	L	1	0	0
M	M	H	1	0	1



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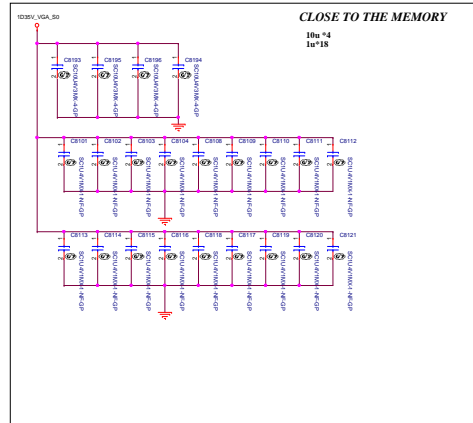
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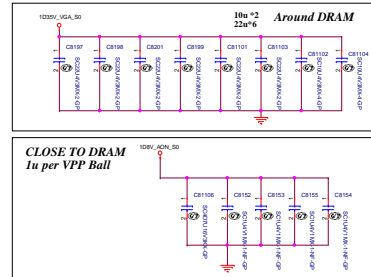


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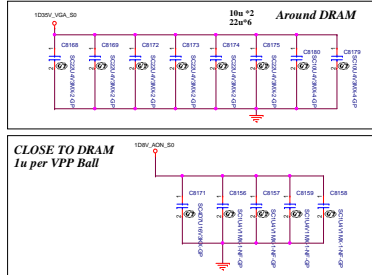
FOR VRAM1



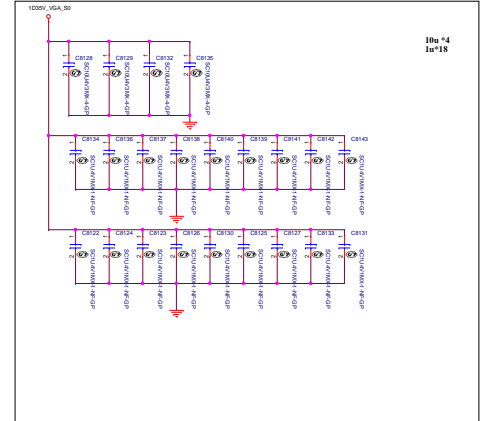
FOR VRAM1

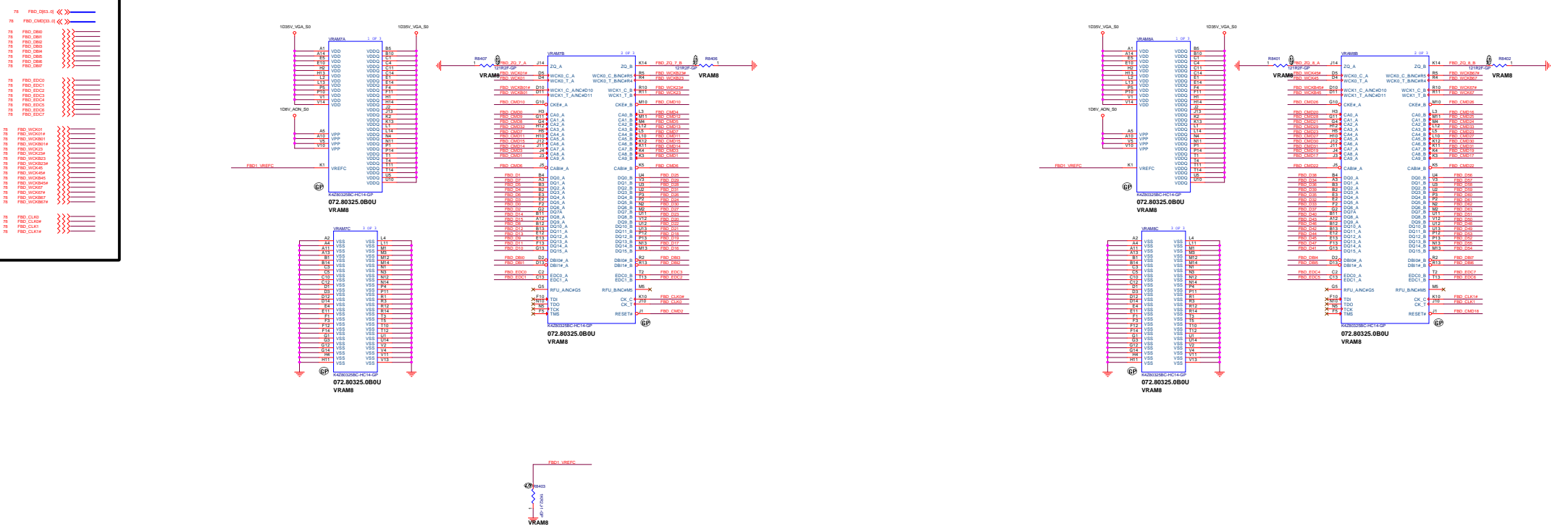


FOR VRAM2



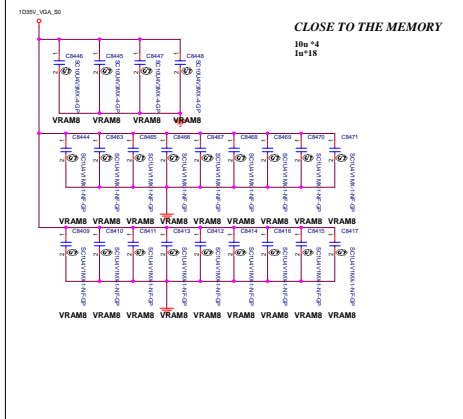
FOR VRAM2



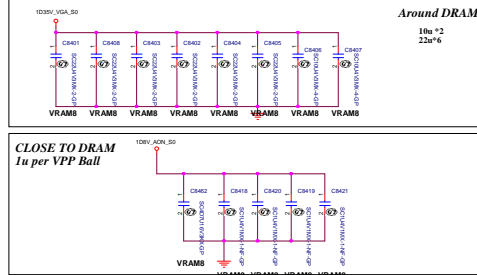


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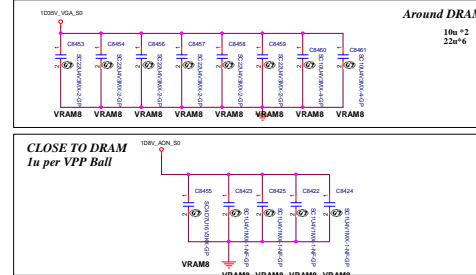
FOR VRAM5



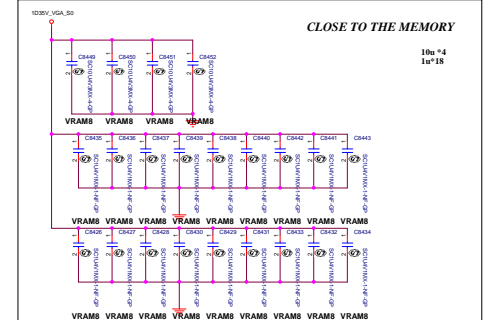
FOR VRAM5



FOR VRAM6



FOR VRAM6



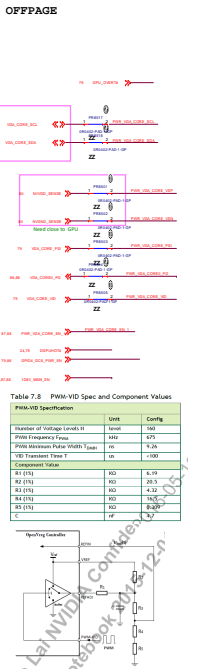
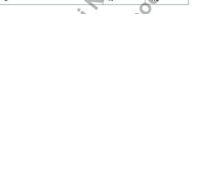
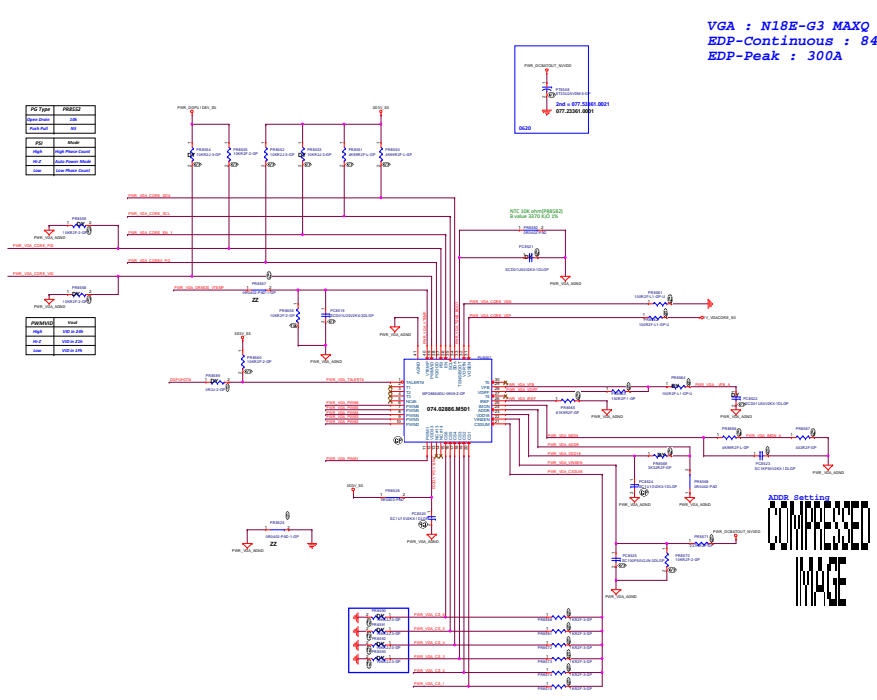


Table 7.9 PWM-VID Spec and Component Values

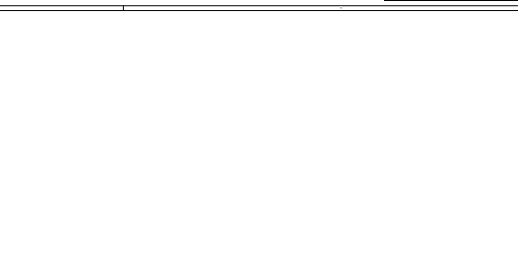
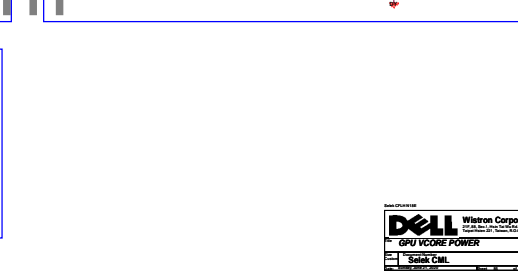
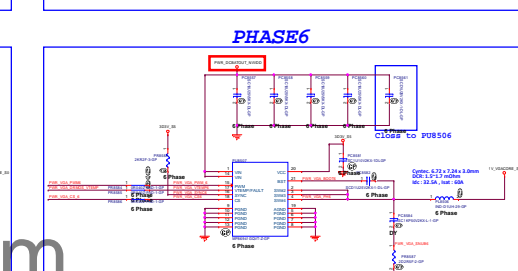
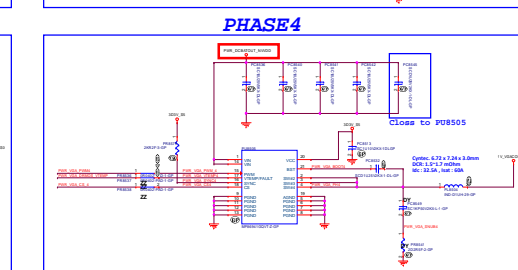
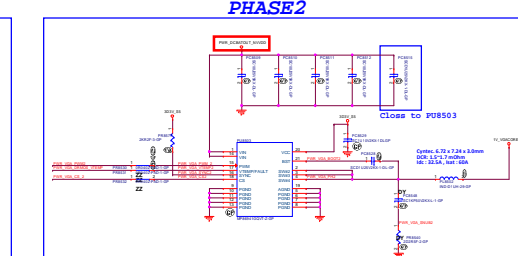
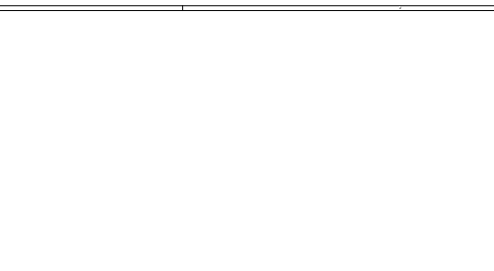
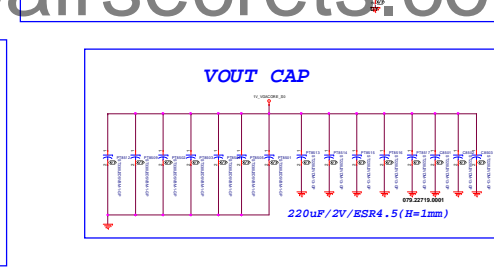
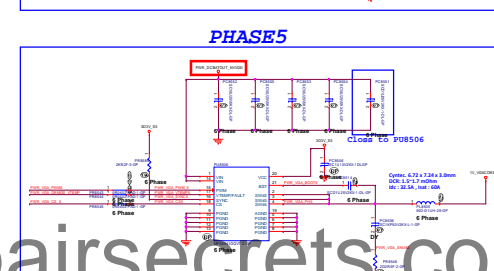
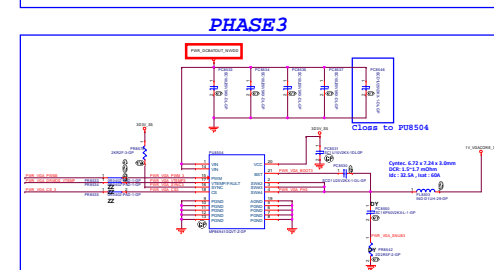
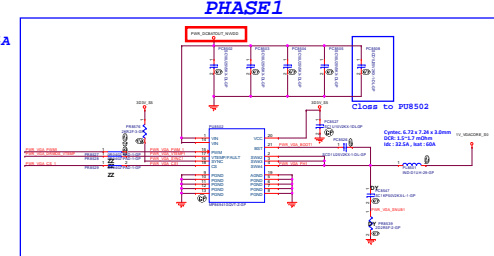
Item	Value	Unit	Config
V _{min}	0.3	V	
V _{max}	1.3	V	
V _{boot}	0.8	V	
Voltage Step Width	6.25	mV	
Number of Voltage Levels (N)	160		
PWM Frequency (F _{pw})	500	kHz	
PWM Minimum Pulse Width (T _{pw})	10	ns	
VID Transient Time (T _{tr})	100	ns	
Component Value			
R1 (Ω)	10		
R2 (Ω)	10		
R3 (Ω)	10		
R4 (Ω)	10		
R5 (Ω)	10		
C	10	μF	

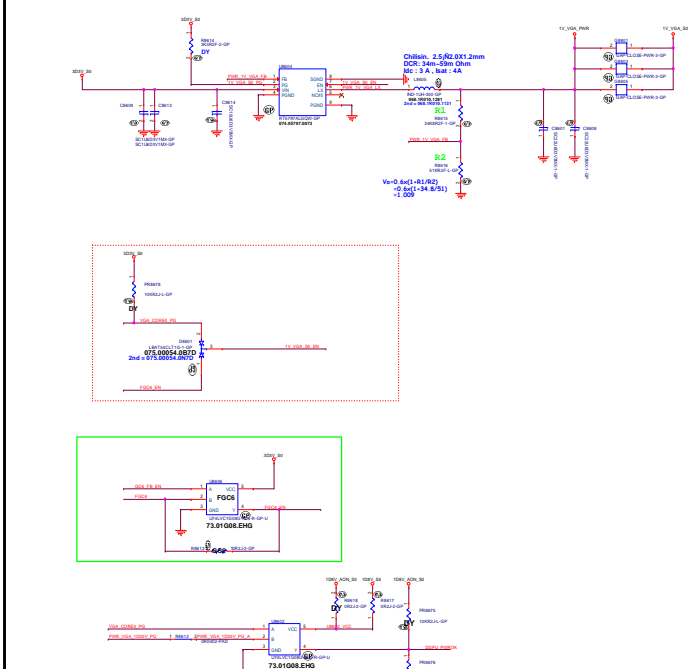


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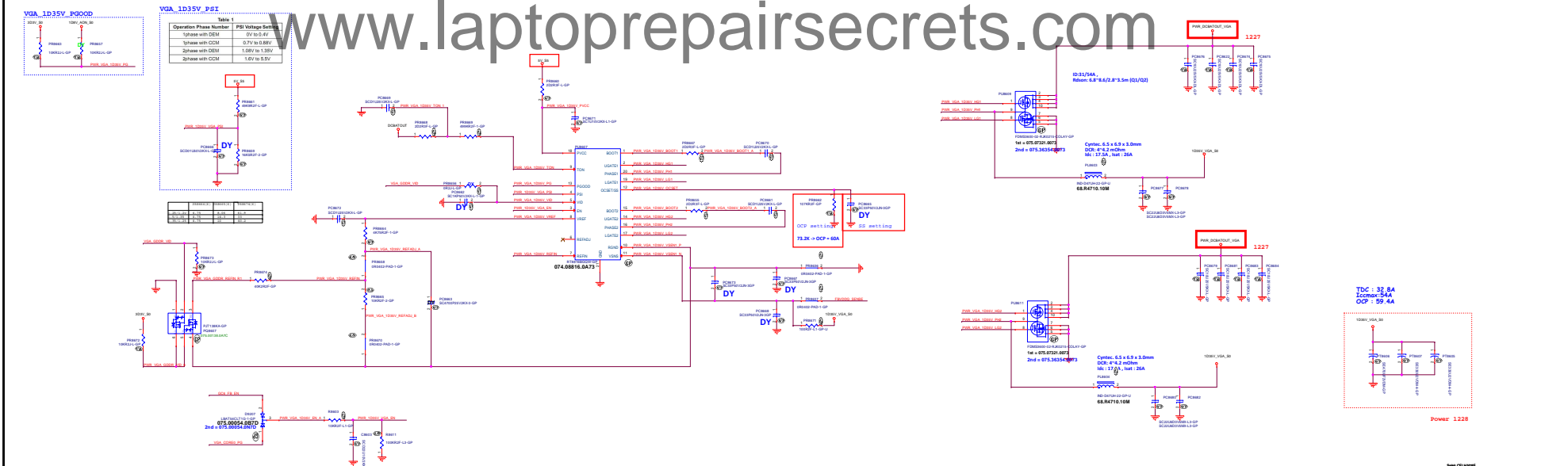
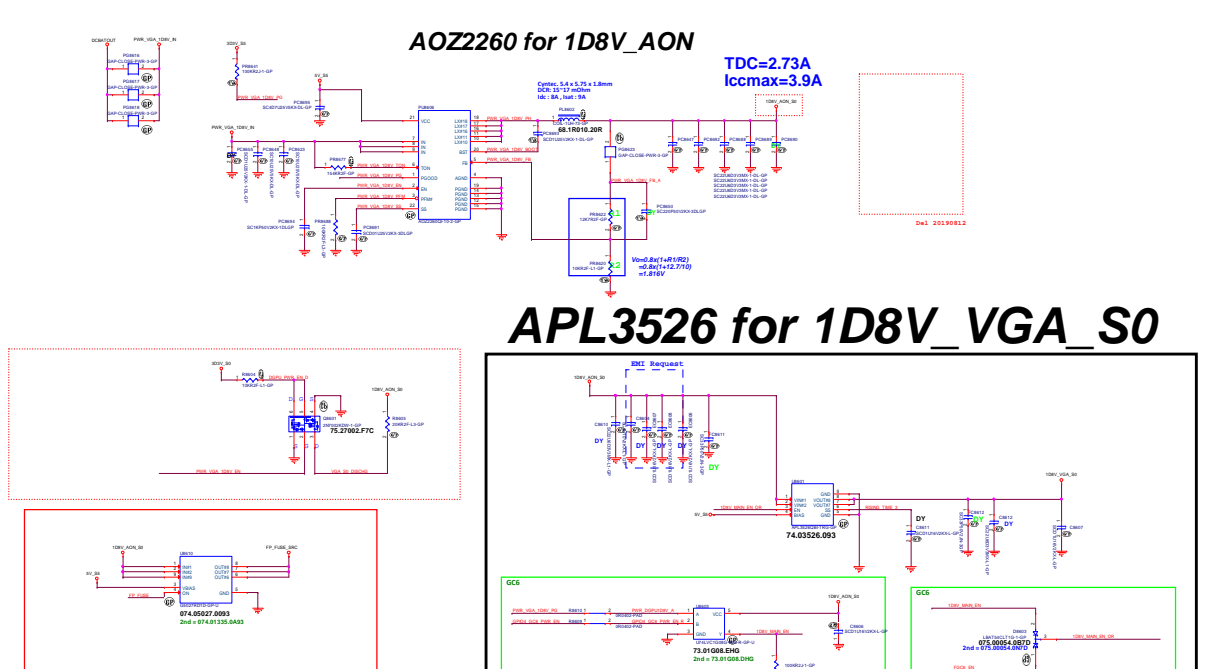





	P8590	P8591	P8592	P8593	PHASE5	PHASE6
6 Phase	DY	DY	DY	DY	attUE	attUE
4 Phase	10k0ba	10k0ba	DY	DY	DY	DY
	10k0ba	10k0ba	10k0ba	10k0ba	DY	DY
	10k0ba	10k0ba	10k0ba	10k0ba	DY	DY





APL3526QB for 1V_VGA_S0



20	DGPU_PWR_EN	
86	PWR_VGA_1D8V_EN	
86	PWR_VGA_1D35V_PG	

From PCH GPIO

From VRAM PG

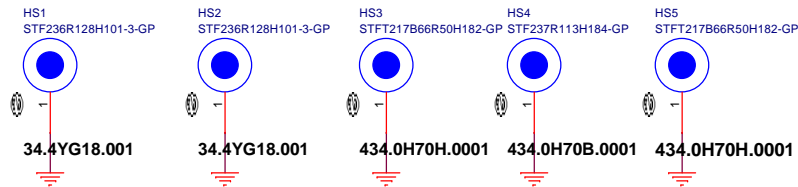
From GPU GPIO

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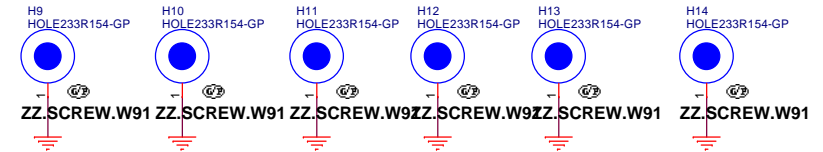
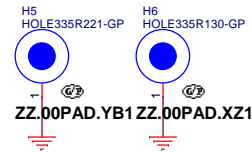
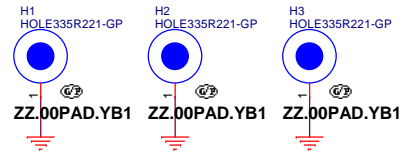
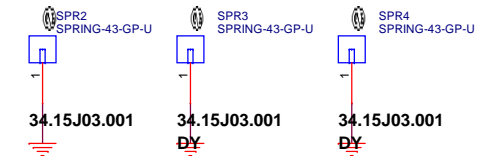
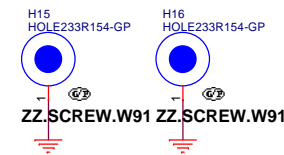
[illegible]

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Rev	A00
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BOM change 434.0H70H.0001

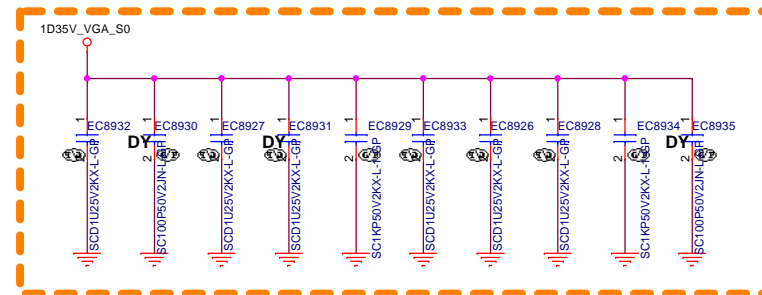
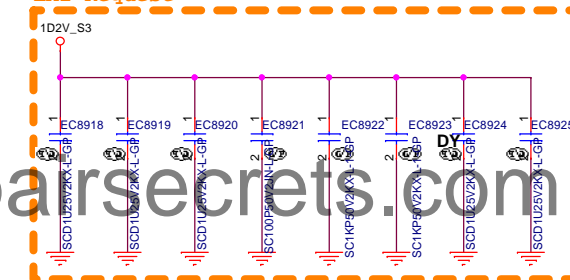
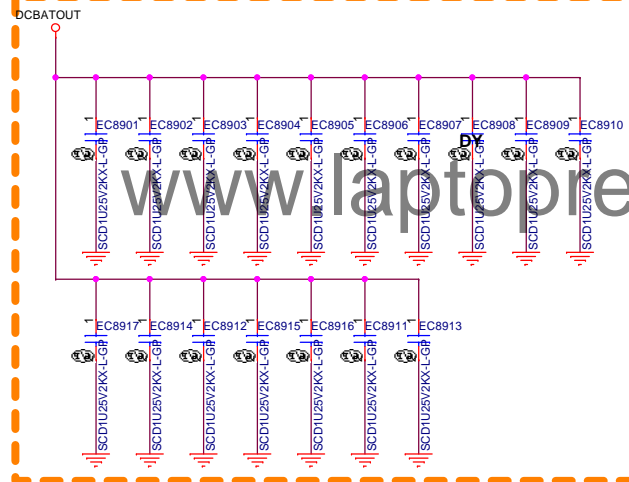
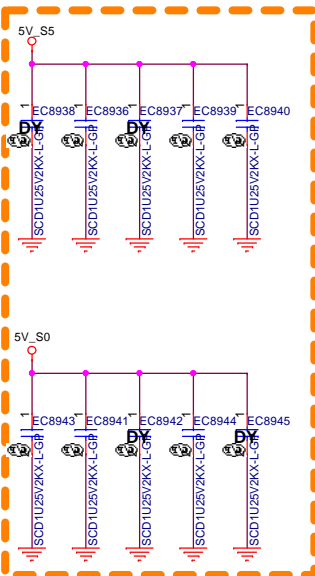


EMI Request

EMI Request

EMI Request


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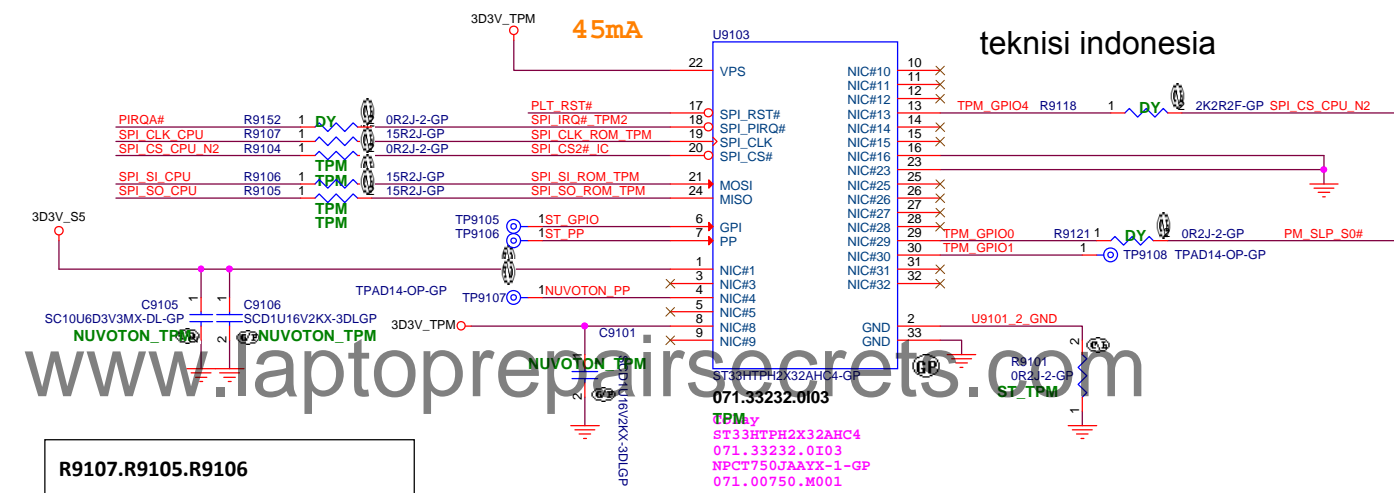
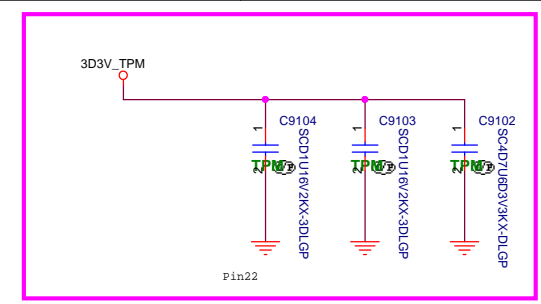
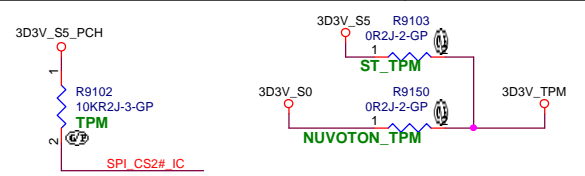
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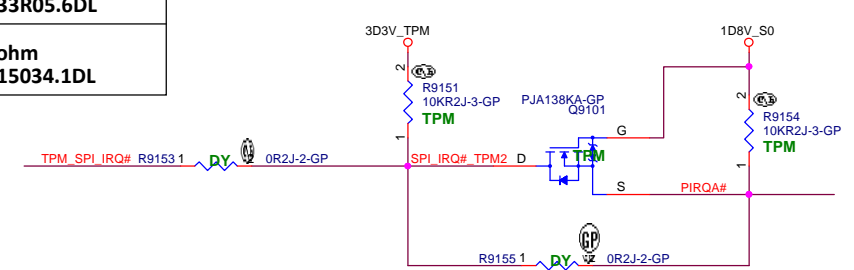
SSID = TPM

5,21,24,25 SPI_SO_CPU <<< _____
15,24,25 SPI_CLK_CPU >>> _____
5,21,24,25 SPI_SI_CPU >>> _____
15 SPI_CS_CPU_N2 <<< _____


15,26,31,61,63,71,79 PLT_RST# >>> _____
15,40 PM_SLP_S0# >>> _____
19 PIRQA# <<< _____
15 TPM_SPI_IRQ# <<< _____



R9107.R9105.R9106	
SPI ROM	33 ohm 64.33R05.6DL
SHARE ROM	15 ohm 63.15034.1DL



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Main Func = XDP

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Wistron Corporation
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TitleCPU_XDP;PCH_XDP

SizeA3


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Title

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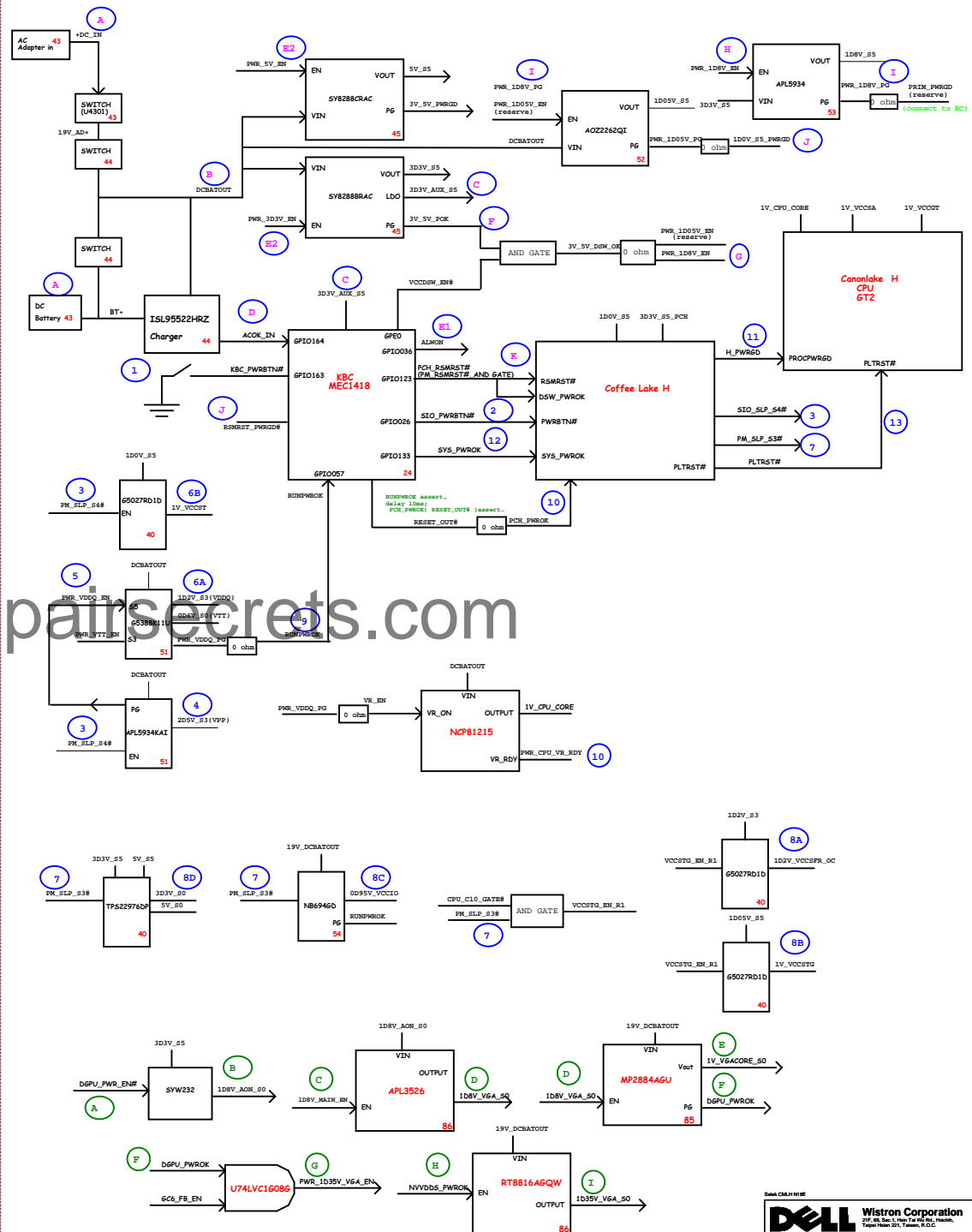
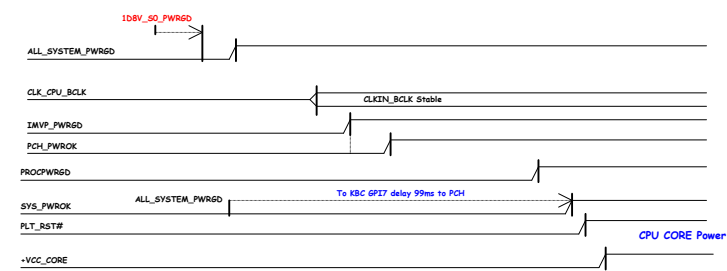
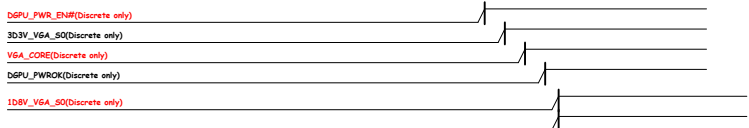
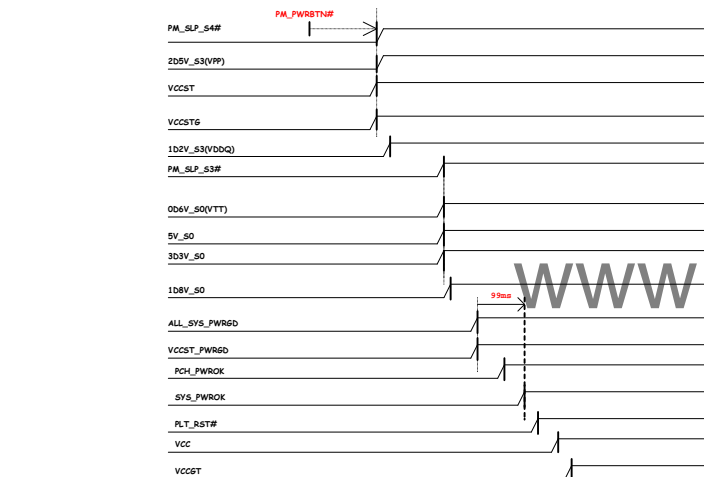
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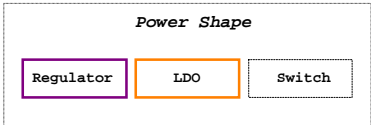
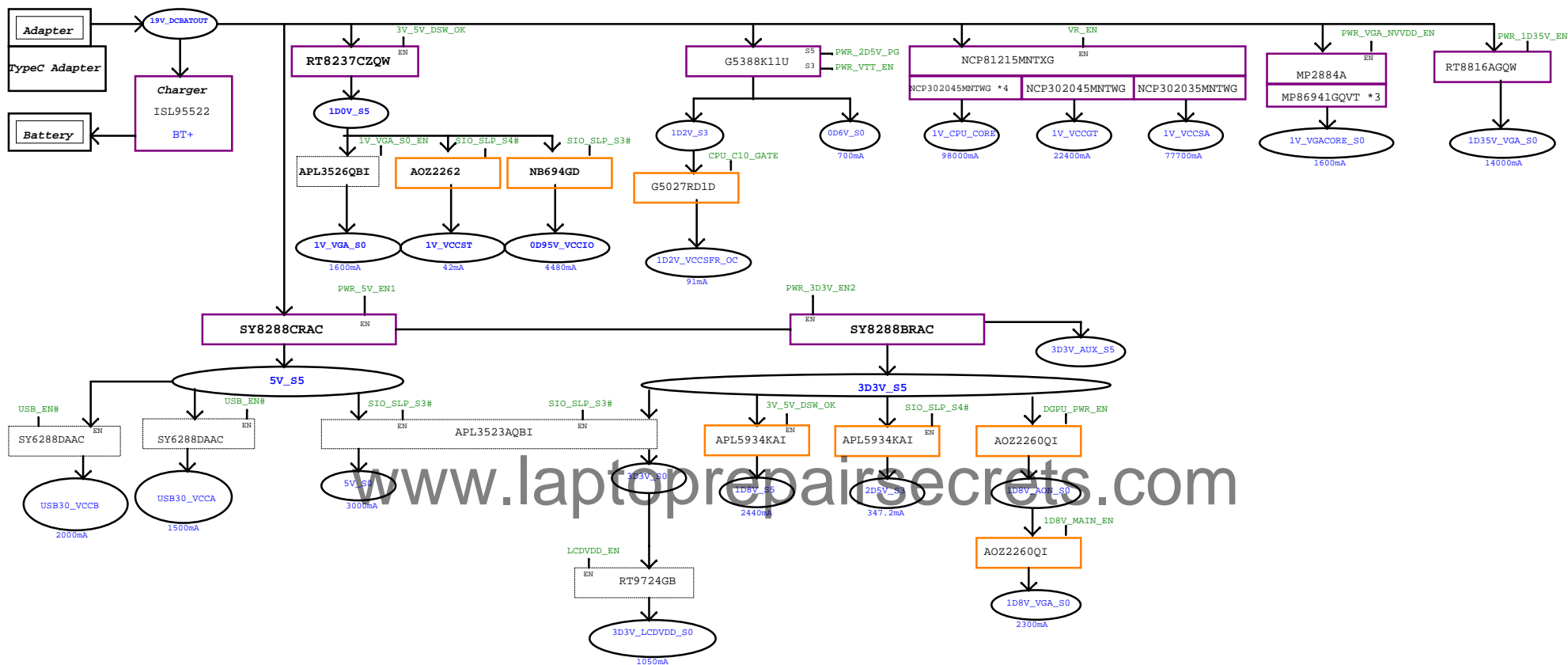
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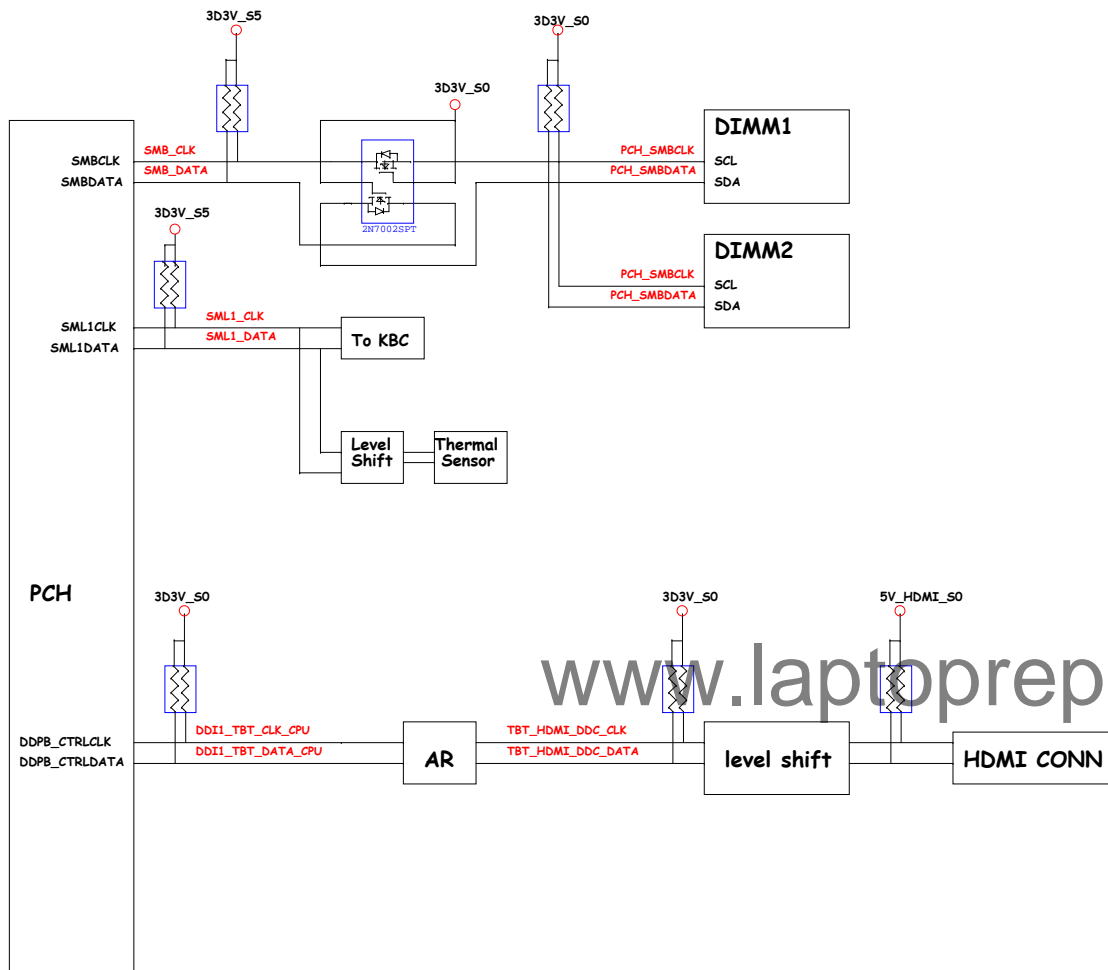
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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3D3V_AUX/5V_AUX (AC mode)

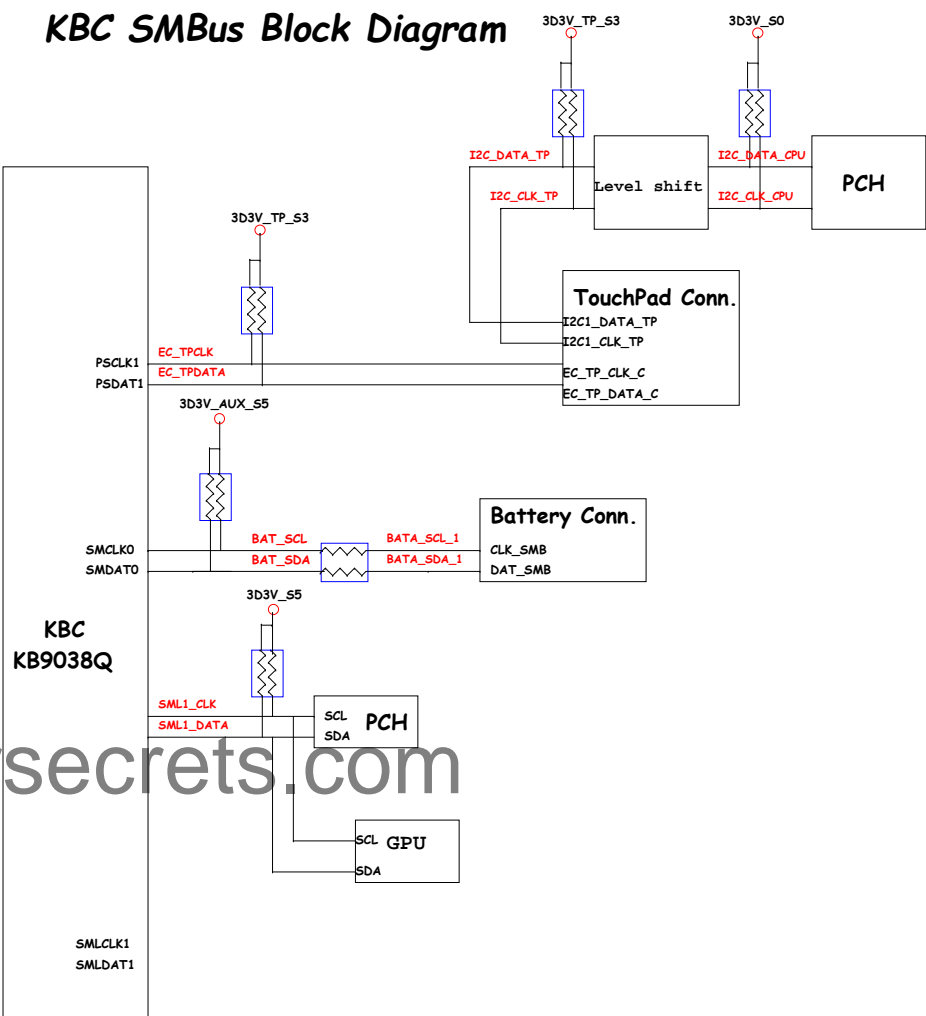




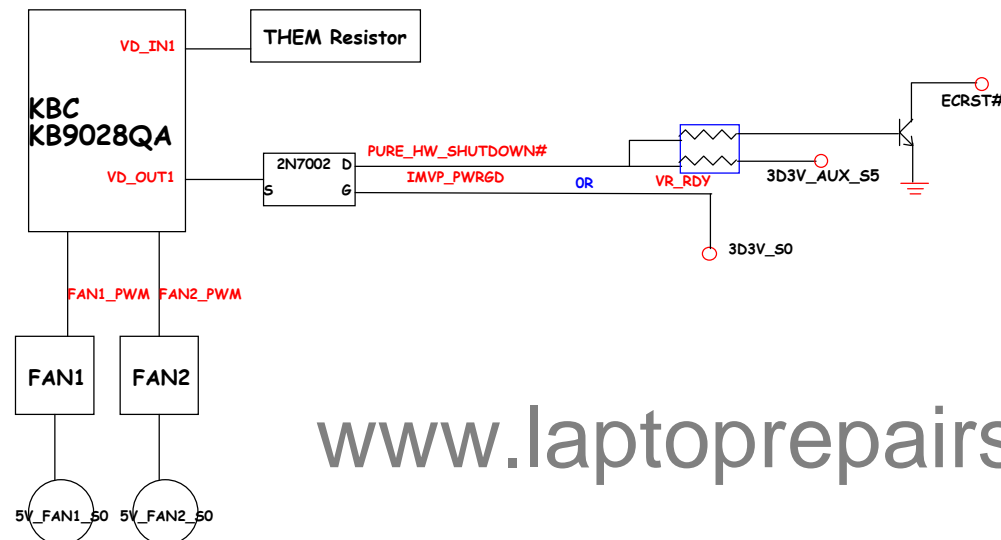
PCH SMBus Block Diagram



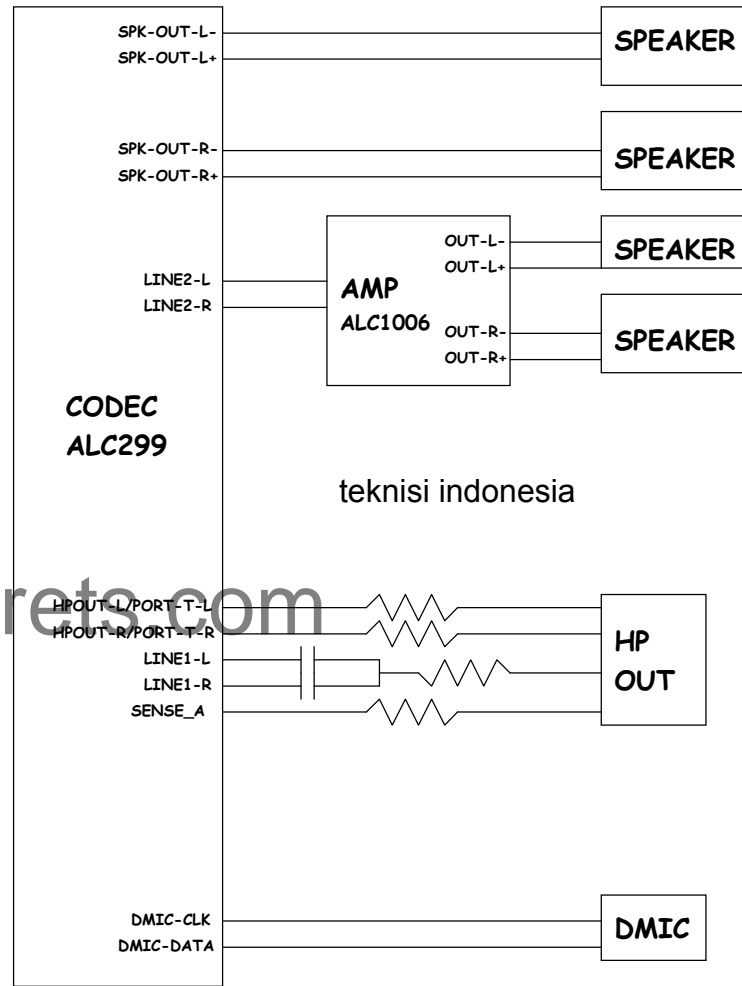
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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